ASSERTION BASED VERIFICATION (ABV) IN VLSI

(Value Added course)

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Course Structure:

Course	Class	No. of students	Duration	Starting Date
Assertion Based Verification	IV. B.Tech	50	3 hrs/week (Maximum of 30 hours)	20.11.2018

Prerequisite:

This course has no specific prerequisites. However some familiarities with the following are especially helpful.

- Verilog/VHDL Programming
- HDL Simulation using EDA tools
- Digital Design Concepts

Course Objectives:

The goal of this course is to familiarize students with the concepts and practical skills required to successfully program and Verify digital systems using HDLs. After finishing the course, students should feel comfortable in building their own digital systems and verifying those using assertions.

About ABV:

Assertion-Based Verification is a methodology for improving the effectiveness of a verification environment in which designers use assertions to capture specific design intent and, either through simulation, formal verification, or emulation of these assertions, verify that the design correctly implements that intent.

With language and tool support for assertions widely available, designers and verification engineers have embraced ABV methodologies to improve design quality and verification productivity. Moreover, designers have found assertions to be invaluable in the debugging process.A comprehensive ABV flow leverages assertion libraries and user-defined assertions that are used in simulation, formal verification, and emulation or FPGA-based prototyping

Topics to be covered:

- Basics of HDL programming
- Programming and Verification using Questasim
- Introduction to ABV
  - Benefits of ABV
  - ABV Methodology
- SystemVerilog Assertions
  - Formal Arguments
  - Local Variables
  - Multiple Clocks
  - Data Integrity
  - Glitch Detection
  - Timing Checks
  - Timing Coverage

Learning References:

http://www.mentor.com/products/fv/methodologies/abv/
https://verificationacademy.com/courses/assertion-based-verification
http://www.cadence.com/products/fv/Pages/abv_flow

Course outcome:

After completion of this course, the student can able to implement assertion based verification using assertions .

Assessment:

1. Every student has to undergo periodic tests.
2. At the end, each student has to give a presentation on a topic covered in this course.