ACADEMIC REGULATIONS

Applicable for students admitted into M.Tech. Programme from 2014-15

The Jawaharlal Nehru Technological University Anantapur shall confer M.Tech. Post graduate degree to candidates who are admitted to the Master of Technology Programmes and fulfill all the requirements for the award of the degree.

1. ELIGIBILITY FOR ADMISSIONS:

Admission to the above programme shall be made subject to the eligibility, qualifications and specialization prescribed by the competent authority for each programme, from time to time.

Admissions shall be made either on the basis of merit rank obtained by the qualifying candidates at an Entrance Test conducted by the University or on the basis of GATE/PGECET score, subject to reservations or policies framed by the Government of Andhra Pradesh policies from time to time.

2. ADMISSION PROCEDURE:

As per the existing stipulations of AP State Council for Higher Education (APSCHE), Government of Andhra Pradesh, admissions are made into the first year as follows

a) Category-A seats are to be filled by Convenor through PGECET/GATE score.

b) Category-B seats are to be filled by Management as per the norms stipulated by Government of A. P.

3. SPECIALIZATION:

The following specializations are offered at present for the M.Tech. programme.

Sl. No.	**Specialization**
1.	CAD/CAM
2	Machine Design
2.	Digital Electronics and Communication Systems
3.	Embedded Systems
4.	VLSI System Design
5.	Computer Science and Engineering
6.	Electrical Power Engineering
7.	Electrical Power Systems
8	Structural Engineering

and any other specialization as approved by the concerned authorities from time to time.

4. COURSE WORK:

4.1. A Candidate after securing admission must pursue the M. Tech. programme of study for four semesters duration.

4.2. Each semester shall be of 20 weeks duration including all examinations.

4.3. A candidate admitted in to the programme should complete it within a period equal to twice the prescribed duration of the programme from the date of admission.

5. ATTENDANCE

5.1. A candidate shall be deemed to have eligibility to write end semester examinations if he has put in at least 75% of attendance aggregate in all subjects/courses in the semester.

5.2. Condonation of shortage of attendance up to 10% i.e., between 65% and above and less than 75% may be granted by the Institute Academic committee.

5.3. Shortage of attendance below 65% in aggregate shall in no case be condoned.

5.4. Condonation of shortage of attendance shall be granted only on genuine and valid reasons on representation by the candidate with supporting evidence.

5.5. A stipulated fee shall be payable towards condonation of shortage of attendance to the institute as per following slab system

1st Slab: Less than 75% attendance but equal to or greater than 70% a normal condonation fee can be collected from the student.

2nd Slab: Less than 70% but equal to or greater than 65%, double the condonation fee can be collected from the student.

5.6. Students whose shortage of attendance is not condoned in any semester are not eligible to take their end examination of that class and their registration shall stand cancelled for that semester.

5.7. A student will not be promoted to the next semester unless he satisfies the attendance requirements of the current semester, as applicable.

5.8. A student detained due to shortage of attendance, will have to repeat that semester when offered next.

6. CREDIT SYSTEM NORMS:

TABLE 1

	Period(s)/week	**Credits**
Theory	01	01
Practical	03	02
Seminar	01	01
Project	-	16

7. EVALUATION:

7.1 Distribution of marks

S. No	Examination	Marks	Examination and Evaluation	Scheme of Evaluation
1.	Theory	60	Semester-end examination (External evaluation)	The question paper shall be of descriptive type with 5 questions with internal choice are to be answered in 3hours duration of the examination.
		40	Mid - Examination of 120 Min. duration (Internal evaluation). 4 descriptive type questions with internal choice are to be answered and evaluated for 30 marks, and the reaming 10 marks are to be allotted for 3-5 assignments to be submitted by the student. The assignment marks are to be awarded based on the completeness of the assignment, correctness of the assignment and in-time submission, evaluated for 10 marks and average of the total assignment marks are rounded to the next integer.	Two mid-exams 30 marks each are to be conducted. Better one to be considered. **Mid-I:** After first spell of instructions (I&II Units). **Mid-II:** After second spell of instructions (III - V Units).

S. No	Examination	Marks	Examination and Evaluation		Scheme of Evaluation
2	Laboratory	60	Semester-end Lab Examination (External evaluation)		**For laboratory courses: 3** hours duration. One External and One Internal examiners.
		40	30	Day to Day evaluation (Internal evaluation)	Performance in laboratory experiments.
			10	Internal evaluation	Practical Tests (one best out of two tests includes viva-voce)
3	Seminar in each of the semesters. 2 hours /week	100	Internal Evaluation 20 Marks for Report 20 Marks for subject content 40 Marks for presentation 20 Marks for Question and Answers		Continuous evaluation during a semester by the Departmental Committee (DC)
4	Project work	Grade A (95%) Grade B (85%)	12 credits	External evaluation	End Project Viva-Voce Examination by Committee as detailed under sect. 9.
			4 credits	Internal evaluation	Continuous evaluation by the DC. as detailed under sect. 9.5

7.2 A candidate shall be deemed to have secured the minimum academic requirement in a subject/practical if he secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

7.3 A candidate has to secure a minimum of 50% to be declared successful.

7.4 In case the candidate does not secure the minimum academic requirement in any of the subjects/practical, he has to reappear for the Examination either supplementary or regular in that subject/practical along with the next batch students. A separate supplementary examinations will be conducted for the I semester students at the end of II semester.

7.5 **Revaluation / Recounting:** Students shall be permitted to request for recounting/ revaluation of the end theory examination answer scripts within a stipulated period after payment of prescribed fee. After recounting or revaluation, records are updated with changes if any and the student will be issued a revised memorandum of marks. If there are no changes, the student shall be intimated the same through a letter or a notice.

8. RE-REGISTRATION FOR IMPROVEMENT OF INTERNAL EVALUATION MARKS(for theory subjects only):

8.1 Out of the subjects the candidate has failed in the examination due to internal evaluation marks secured being less than 50%, the candidate shall be given one chance for each theory subject and for a maximum of **Three** theory subjects for improvement of internal evaluation marks.

8.2 The candidate can re-register for the chosen subjects and fulfill the academic requirements. Re-registration shall not be permitted after the commencement of class work for that semester. The candidate can re-register for 1st semester subjects when he is in his 3rd semester and for 2nd semester subjects when he is in his 4th semester else the candidate can re-register after completion of 2 years course work.

8.3 For each subject re-registered, the candidate has to pay a fee equivalent to one third of the semester tuition fee.

8.4 In the event of re-registration, the internal evaluation marks as well as the End Examinations marks secured in the previous attempt(s) for those subjects stand cancelled.

9. EVALUATION OF PROJECT WORK:

Every candidate shall be required to submit thesis/dissertation after taking up a topic approved by the Departmental Committee.

9.1 The Departmental Committee (DC) consisting of HOD, Project supervisor and two internal senior experts shall monitor the progress of the project work. A Project Review Committee (PRC) shall be

constituted with Principal as Chair Person, Heads of the departments of the M.Tech Programs and Two other senior faculty members, as members of the PRC. PRC will come into action when the DC is not able to resolve the issues.

9.2 Registration of Project work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the courses (theory, practical and seminar of I & II semesters).

9.3 After satisfying 9.2, a candidate has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work to the DC for approval. Only after obtaining the approval of DC, the student can initiate the project work.

9.4 The work on the project shall be initiated in the penultimate semester and continued in the final semester. The duration of the project is for two semesters. The candidate can submit Project thesis with the approval of DC after 36 weeks from the date of registration at the earliest but not later than one calendar year from the date of registration for the project work. Extension of time within the total permissible limit for completing the programme is to be obtained from the Head of the Institution.

9.5 The Internal Evaluation shall be made by the DC to grade, on the basis of two seminars presented by the student on the topic of his project.

9.6 The student must submit status report at least in two different phases during the project work period. These reports must be approved by the DC before submission of the Project Report.

9.7 A candidate shall be allowed to submit the thesis / dissertation only after passing all the prescribed subjects (theory, practical, seminar and project work internal evaluation).

9.8 A candidate has to prepare four copies of the thesis/dissertation certified in the prescribed format by the supervisor and HOD. Out of which three copies shall be submitted in the examination section.

9.9 Viva-voce examination shall be conducted by a board consisting of the supervisor, Head of the department and the examiner. The board shall jointly report candidate's work as.

A Very Good performance
B Moderate Performance
C Failure Performance

Head of the Department shall coordinate and make arrangements for the conduct of viva-voce.

If the report of the viva-voce is failure performance, the candidate will retake the viva-voce examination after three months. If he fails to get a satisfactory report at the second viva-voce examination, he will not be eligible for the award of the degree.

10. CREDIT POINT AVERAGE AND CUMULATIVE CREDIT POINT AVERAGE:

10.1. CREDIT POINT AVERAGE (CPA):

$$\textbf{CPA} = \frac{\sum_i C_i T_i}{10 \sum_i C_i}$$

Where C_i= Credits earned for Course i in any semester/year.

T_i= Total marks obtained for course i in any semester/year.

10.2. CUMULATIVE CREDIT POINT AVERAGE (CCPA):

$$\textbf{CCPA} = \frac{\sum_n \sum_i C_{ni} T_{ni}}{10 \sum_n \sum_i C_{ni}}$$

Where ***n*** refers to the semester in which such courses were credited.

The CCPA is awarded only when a student earns all the credits prescribed for the programme.

10.3. OVERALL PERFORMANCE:

CCPA	Classification of Final Results
7.0 and above	First Class with Distinction
6.0 and above but below 7.0	First Class
5.0 and above but below 6.0	Second Class

11. TRANSCRIPTS:

After successful completion of the entire programme of study, a transcript containing performance of all the academic years will be issued as a final record. Duplicate transcripts will be issued if required, after payment of requisite fee. Partial transcript will also be issued up to any point of study to a student on request.

12. ELIGIBILITY:

A student shall be eligible for the award of M.Tech Degree if he fulfills all the following conditions:

i. Registered and successfully completed all the components prescribed in the programme of study to which he was admitted.

ii. Successfully acquired all **72 credits** as specified in the curriculum corresponding to the branch of his study within the stipulated time.

iii. No disciplinary action is pending against him.

13. AWARD OF DEGREE:

The Degree will be conferred and awarded by Jawaharlal Nehru Technological University Anantapur, Anantapur on the recommendations of the Principal, AITS (Autonomous) based on the eligibility as mentioned in clause 11.

14. WITHHOLDING OF RESULTS:

If the candidate has any dues to the Institute or if any case of in-discipline is pending against him, the result of the candidate shall be withheld and he will not be allowed / promoted into the next higher semester. The issue of degree is liable to be withheld in such cases.

15. TRANSITORY REGULATIONS:

Candidates who have discontinued or have been detained for want of attendance or who have failed after having undergone the course in earlier regulations and wish to continue the course are eligible for admission into the unfinished semester from the date of commencement of class work with the same or equivalent subjects as and when subjects are offered. Whereas, he continues to be in the academic regulations he was first admitted.

16. AMENDMENTS OF REGULATIONS:

The Chairman, Academic Council of Annamacharya Institute of Technology and Sciences, Rajampet (Autonomous) reserves the right to revise, amend, or change the Regulations, Scheme of Examinations and/or Syllabi or any other policy relevant to the needs of the society or industrial requirements etc., without prior notice.

17. GENERAL:

Where the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”, “hers”.

18. Any legal issues are to be resolved in Rajampet Jurisdiction.

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Annamacharya Institute of Technology and Sciences, Rajampet.	
Curriculum for the Programmes under Autonomous Scheme	
Regulation	R 2014
Department	Department of Electronics and Communication Engineering
Programme Code & Name	PA: M.Tech. Digital Electronics and Communication Systems

Semester I

Course Code	Course Name	Hours/ Week		Credit	Maximum marks		
		L	P	C	Internal	External	Total
4PA311	Digital System Design	4	0	4	40	60	100
4PA312	Advanced Digital Signal Processing	4	0	4	40	60	100
4PA313	Digital Communication Techniques	4	0	4	40	60	100
4PA314	Wireless Communications	4	0	4	40	60	100
4PC314	Modelling and synthesis through verilog HDL	4	0	4	40	60	100
	Elective – I	4	0	4	40	60	100
4PA316	Seminar – I	0	0	2	100	00	100
4PA317	Digital Design Laboratory	0	3	2	40	60	100
Total		24	3	28	800		

Semester II

Course Code	Course Name	Hours/ Week		Credit	Maximum marks		
		L	P	C	Internal	External	Total
4PA321	Coding Theory and Techniques	4	0	4	40	60	100
4PA322	High Speed Networks	4	0	4	40	60	100
4PA323	Micro computer System Design	4	0	4	40	60	100
4PA324	Detection and Estimation of Signals	4	0	4	40	60	100
4PA325	Image and Video Processing	4	0	4	40	60	100
	Elective – II	4	0	4	40	60	100
4PA327	Seminar – II	0	0	2	100	00	100
4PA328	Advanced Communications Laboratory	0	3	2	40	60	100
Total		24	3	28	800		

Semester III & IV

Course Code	Course Name	Credit	Maximum Marks		
		C	Internal	External	Total
4PA331	**PROJECT WORK**	16	**GRADE (A/B/C)**		

List of Electives

Elective – I	4PA318	Advanced Computer Architectures
	4PA315	System Modeling and Simulation
	4PB311	Embedded System Concepts
Elective – II	4PB324	DSP Processors and Architectures
	4PA329	Neural Networks & Applications
	4PA326	Compression Techniques

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES::RAJAMPET
(AN AUTONOMOUS INSTITUTION)
M.Tech (D E C S) I Semester

DIGITAL SYSTEM DESIGN

UNIT I

DESIGN OF DIGITAL SYSTEMS: ASM charts, Hardware description language and control sequence method, Reduction of state tables, state assignments.

SEQUENTIAL CIRCUIT DESIGN: design of Iterative circuits, design of sequential circuits using ROMs and PLAs.

UNIT II

FAULT MODELING: Fault classes and models – Stuck at faults, bridging faults, transition and intermittent faults.

TEST GENERATION: Fault diagnosis of Combinational circuits by conventional methods – Path Sensitization technique, Boolean difference method, Kohavi algorithm. D – Algorithm, PODEM, Random testing, transition count testing, Signature analysis and testing for bridging faults.

UNIT III

FAULT DIAGNOSIS IN SEQUENTIAL CIRCUITS: State identification and fault detection experiment. Machine identification, Design of fault detection experiment.

UNIT IV

PROGRAMMING LOGIC ARRAYS & TESTING: Design using PLA's, PLA minimization and PLA folding. Fault models, Test generation and Testable PLA design.

UNIT V

ASYNCHRONOUS SEQUENTIAL MACHINE: fundamental mode model, flow table, state reduction, minimal closed covers, races, cycles and hazards.

TEXTBOOKS

1. Z. Kohavi – "Switching & finite Automata Theory" (TMH)
2. N. N. Biswas – "Logic Design Theory" (PHI)
3. Nolman Balabanian, Bradley Calson – "Digital Logic Design Principles" – Wiley Student Edition 2004.

REFRENCES

1. M. Abramovici, M. A. Breues, A. D. Friedman – "Digital System Testing and Testable Design", Jaico
Publications
2. Charles H. Roth Jr. – "Fundamentals of Logic Design".
3. Frederick. J. Hill & Peterson – "Computer Aided Logic Design" – Wiley 4th Edition.

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES::RAJAMPET
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M.Tech (D E C S) I Semester

ADVANCED DIGITAL SIGNAL PROCESSING

UNIT I

INTRODUCTION: Discrete-Time Signals, Sequences and sequence Representation, Discrete-Time Systems, Time-Domain Characterization and Classification of LTI Discrete-Time Systems. The Continuous-Time Fourier Transform, The discrete-Time Fourier Transform, energy Density Spectrum of a Discrete-Time Sequence, Band-Limited Discrete-Time signals, The Frequency Response of LTI Discrete-Time System. Complementary Transfer Function. Inverse Systems, System Identification, Digital Two-Pairs.

UNIT II

DIGITAL FILTER SRTUCTURE AND DESIGN: All pass filters, Tunable IIR Digital Filter, Polyphase Structures, Digital Sine-Cosine Generator, Computational Complexity of Digital Filter Structures, Design of IIR Filter using pade approximation, Least Square Design Methods, Design of Computationally Efficient FIR Filters.

UNIT III

DSP ALGORITHEMS: Fast DFT algorithms based on Index mapping, Sliding Discrete Fourier Transform, DFT Computation Over a narrow Frequency Band, Split Radix FFT, Linear filtering approach to Computation of DFT using Chirp Z-Transform.

UNIT IV

NON PARAMETRIC&PARAMETRIC METHODS FOR POWER SPECTRUM ESTIMATION: Barlett and weltch methods. Relation between auto correlation & model parameters, Yule-Waker & Burg Methods, MA & ARMA models for power spectrum estimation.

UNIT V

MULTI RATE SIGNAL PROCESSING: Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Filter design & Implementation for sampling rate conversion.

TEXTBOOKS:

1. Digital Signal Processing by Sanjit K Mitra, Tata MCgraw Hill Publications.
2. Digital Signal Processing Principles, Algorithms, Applications by J G Proakis, D G Manolokis, PHI.
3. Digital Signal Processing Emmanuel C Ifeachor, Barrie W Jrevis, Pearson Education

REFERENCES:

1. Discrete-Time Signal Processing by A V Oppenhiem, R W Schafer, Pearson Education.
2. DSP- A Practical Approach- Emmanuel C Ifeacher Barrie. W. Jervis, Pearson Education.
3. Modern spectral Estimation techniques by S. M .Kay, PHI, 1997
4. Theory and Applications of DSP L.R Rabiner and B gold

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES::RAJAMPET
(AN AUTONOMOUS INSTITUTION)
M.Tech (D E C S) I Semester

DIGITAL COMMUNICATION TECHNIQUES

UNIT I INTRODUCTION: Probability-Random variables – Probability Density Functions – Gaussian, Rayleigh, Rician, and Binomial - Chebyshev's inequality – Random Processes – Classification of Random Processes.Signal space representations- Vector Space Concepts, Signal Space Concepts, Orthogonal Expansion of Signals – Gram-Schmidt Procedure

UNIT II DIGITAL MODULATION SCHEMES AND AWGN: Memory less Modulation Methods – PAM, Phase Modulation, QAM – Multidimensional Signaling – Signaling Schemes with Memory- CPFSK,CPM, Waveform & Vector AWGN Channel – Optimal Detection for the vector AWGN Channel – Implementation of Optimum Receiver for AWGN Channel

UNIT III FADING CHANNELS: Characterization of fading multipath channels - Statistical Models for fading channels – Frequency-non Selective slowly fading channels – Rayleigh & Nakagami fading – Diversity Techniques for fading Multipath Channels, RAKE Demodulator & Performance – Generalised RAKE demodulator- A tapped delay line channel modulator.

UNIT IV COMMUNICATION OVER BAND LIMITED CHANNELS: Characterization of band limited Channels- Signal design for Band limited channel - Nyquist criterion for zero ISI, partial response signaling- Equalization Techniques- linear Equalization: Peak Distortion and MSE, Decision feedback equalization.

UNIT V ORTHOGONAL FREQUENCY DIVISION MULTIPLEXING (OFDM): Introduction to OFDM, Modulation & Demodulation in OFDM – FFT algorithm implementation of OFDM System – Filter bank implementation of of OFDM Receiver.

TEXT BOOKS:

1. J. Proakis, Masoud salehi, Digital Communications, McGraw Hill, Fifth edition, 2008.
2. Herbert Taub, Donald Schilling, Gowtham Saha , Principles of Communications Systems, 3rd Edition TMH, 2008.

REFERENCE BOOKS:

1. Ahmad R S Bahai ,Burton R Saltzberg ,Mustafa Ergen, "Multi-carrier Digital Communications: Theory and Applications of OFDM." Springer Publications.
2. Edward. A. Lee and David. G. Messerschmitt, "Digital Communication", Allied Publishers (second edition).
3. J Marvin.K.Simon, Sami. M. Hinedi and William. C. Lindsey, "Digital Communication Techniques", PHI.
4. William Feller, "An introduction to Probability Theory and its applications", Vol 11, Wiley 2000.

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES::RAJAMPET
(AN AUTONOMOUS INSTITUTION)
M.Tech (D E C S) I Semester
WIRELESS COMMUNICATIONS

UNIT I

INTRODUCTION TO WIRELESS COMMUNICATIONS SYSTEMS AND STANDARDS :

Evolution of mobile radio communications, Examples of Wireless Communication systems, Comparison, Second Generation Cellular Networks, Third Generation Cellular Networks , Wireless Local Loop(WLL), Bluetooth and Personal Area Networks.

UNIT II

MOBILE RADIO PROPAGATION:

Large-Scale Path Loss: Introduction to Radio Wave Propagation, Free Space Propagation Model, Relating power to electric field, the three basic Propagation Mechanisms, Reflection, Ground Reflection (Two-Ray) Model, Diffraction, Scattering.

Small-Scale Fading and Multipath: Small scale multipath propagation, Impulse Response Model of a Multipath Channel, Small-Scale Multipath Measurements.

UNIT III

DIVERSITY AND SPREAD SPECTRUM MODULATION TECHNIQUES:

Derivation of selection diversity and maximal ratio combining improvement, Polarization diversity, Frequency diversity, Time diversity, RAKE Receiver, Pseudo-Noise (PN) sequences, Direct sequence spread spectrum (DS-SS), Frequency Hopped spread spectrum (FH-SS), Performance of Direct sequence spread spectrum and Frequency Hopped spread spectrum.

UNIT IV

MULTIPLE ACCESS TECHNIQUES:

Introduction, Frequency division multiple access, Time division multiple access, Spread spectrum multiple access, Space division multiple access, Capacity of cellular systems: capacity of cellular CDMA, capacity of CDMA with multiple cells, capacity of space division multiple access

UNIT V

CAPACITY OF WIRELESS CHANNELS AND MULTIPLE ANTENNAS:

Capacity in AWGN, Capacity of flat fading channels, Capacity of frequency selective fading channels Multiple Input Multiple output (MIMO) systems- Narrow band MIMO model, Parallel Decomposition of the MIMO Channel, MIMO channel capacity: Static channels, fading channels.

TEXT BOOKS:

1. Theodore.S. Rappaport, "Wireless Communication, principles & practice", 2nd Edition, Pearson
2. Andrea Goldsmith, "Wireless Communications", Cambridge University press-2005

REFERENCES:

1. Kamilo Feher, 'Wireless digital communication', PHI, 1995.
2. John G.Proakis."Digital Communication",4th edition
3. A.J.Viterbi, "CDMA- Principles of Spread Spectrum", Addison Wesley, 1995.

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES::RAJAMPET
(AN AUTONOMOUS INSTITUTION)
M.Tech (D E C S) I Semester

MODELLING AND SYNTHESIS THROUGH VERILOG HDL

UNIT I

HARDWARE MODELING WITH THE VERILOG HDL : Hardware Encapsulation -The Verilog Module, Hardware Modeling Verilog Primitives, Descriptive Styles, Structural Connections, Behavioral Description In Verilog, Hierarchical Descriptions of Hardware, Structured (Top Down) Design Methodology, Arrays of Instances, Using Verilog for Synthesis, Language Conventions, Representation of Numbers, Verilog Variables, Logic Value Set, Data Types, Strings, Constants, Operators, Expressions and Operands, Operator Precedence.

UNIT II

LOGIC SYSTEM MODELING IN VERILOG HDL: User-Defined Primitives, User Defined Primitives – Combinational Behavior User-Defined Primitives –Sequential Behavior, Initialization of Sequential Primitives. Models Of Propagation Delay; Built-In Constructs for Delay, Signal Transitions, Verilog Models for Gate Propagation Delay (Inertial Delay), Time Scales for Simulation, Verilog Models for Net Delay (Transport Delay), Module Paths and Delays, Path Delays and Simulation, Inertial Delay Effects and Pulse Rejection.

UNIT III

SWITCH-LEVEL MODELS IN VERILOG:MOS Transistor Technology, Switch Level Models of MOS Transistors, Switch Level Models of Static CMOS Circuits, Alternative Loads and Pull Gates, CMOS Transmission Gates. Bio-Directional Gates (Switches), Signal Strengths, Ambiguous Signals, Strength Reduction By Primitives, Combination and Resolution of Signal Strengths, Signal Strengths and Wired Logic.

BEHAVIORAL DESCRIPTIONS IN VERILOG HDL: Verilog Behaviors, Behavioral Statements, Procedural Assignment, Procedural Continuous Assignments, Procedural Timing Controls and Synchronization, Intra-Assignment, Delay-Blocked Assignments, Non-Blocking Assignment, Intra-Assignment Delay: Non-Blocking Assignment, Simulation of Simultaneous Procedural Assignments, Repeated Intra Assignment Delay, Indeterminate Assignments and Ambiguity, Constructs for Activity Flow Control, Tasks and Functions, Summary of Delay Constructs in Verilog, System Tasks for Timing Checks, Variable Scope Revisited, Module Contents, Behavioral Models of Finite State Machines.

UNIT IV

SYNTHESIS OF COMBINATIONAL AND SEQUENTIAL LOGIC: HDL-Based Synthesis, Technology-Independent Design, Benefits of Synthesis, Synthesis Methodology, Vendor Support, Styles for Synthesis of Combinational Logic, Technology Mapping and Shared Resources, Three State Buffers, Three State Outputs and Don’t Cares.

Synthesis of Sequential Logic Synthesis of Sequential Udps, Synthesis of Latches, Synthesis of Edge-Triggered Flip Flops, Registered Combinational Logic, Shift Registers and Counters, Synthesis of Finite State Machines, Resets, Synthesis of Gated Clocks, Design Partitions and Hierarchical Structures.

UNIT V

SYNTHESIS OF LANGUAGE CONSTRUCTS: Synthesis of Nets, Synthesis of Register Variables, Restrictions on Synthesis of "X" and "Z", Synthesis of Expressions and Operators, Synthesis of Assignments, Synthesis of Case and Conditional Statement, Synthesis of Resets, Timings Controls in Synthesis, Synthesis of Multi-Cycle Operations, Synthesis of Loops, Synthesis if Fork Join Blocks, Synthesis of The Disable Statement Synthesis of User-Defined Tasks, Synthesis of User-Defined Functions, Synthesis of Specify Blocks, Synthesis of Compiler Directives.

TEXT BOOKS:

1. M.D.CILETTI, "Modeling, Synthesis and Rapid Prototyping with the Verilog HDL", Prentice-Hall, 1999.
2. Samir Palanitkar, "Verilog HDL" Pearson Education, 2002.

REFERENCES:

1. M.G.ARNOLD, "Verilog Digital – Computer Design", Prentice-Hall (PTR), 1999.

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES::RAJAMPET
(AN AUTONOMOUS INSTITUTION)
M.Tech (D E C S) I Semester

ADVANCED COMPUTER ARCHITECTURE
(ELECTIVE-I)

UNIT I

FUNDAMENTALS OF COMPUTER DESIGN: Technology trends, cost- measuring and reporting performance quantitative principles of computer design,classifying instruction set- memory addressing- type and size of operands- addressing modes for signal processing- operations in the instruction set, instructions for control flow, encoding an instruction set, the role of compiler

UNIT II

INSTRUCTION LEVEL PARALLELISM (ILP): overcoming data hazards- reducing branch costs, high performance instruction delivery, hardware based speculation, limitation of ILP,ILP SOFTWARE APPROACH: compiler techniques- static branch protection, VLIW approach, H.W support for more ILP at compile time- H.W verses S.W solutions

UNIT III

MEMORY HIERARCHY DESIGN: cache performance, reducing cache misses penalty and miss rate, virtual memory, protection and examples of VM,MULTIPROCESSORS AND THREAD LEVEL PARALLELISM: symmetric shared memory architectures, distributed shared memory, Synchronization, multi threading.

UNIT IV

STORAGE SYSTEMS- Types, Buses, RAID, errors and failures, bench marking a storage device, designing a I/O system.

UNIT V

INTER CONNECTION NETWORKS AND CLUSTERS: interconnection network media, practical issues in interconnecting networks- examples, clusters, designing a cluster

TEXT BOOKS:

1. Computer Architecture A quantitative approach 3rd edition John L. Hennessy & David A. Patterson Morgan Kufmann (An Imprint of Elsevier)

REFERENCES:

1. Kai Hwang and A.Briggs "Computer Architecture and parallel processing", International Edition McGraw-Hill.
2. Dezso Sima, Terence Fountain, Peter Kacsuk, "Advanced Computer Architectures", Pearson.

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES::RAJAMPET
(AN AUTONOMOUS INSTITUTION)
M.Tech (D E C S) I Semester

SYSTEM MODELLING & SIMULATION
ELECTIVE I

UNIT I

Basic Simulation Modeling, Systems, Models and Simulation, Discrete Event Simulation, Simulation of Single Server Queuing System, Simulation of Inventory System, Alternative approach to Modeling and Simulation.

UNIT II

SIMULATION SOFTWARE: Comparison of Simulation Packages with Programming Languages, Classification of Software, Desirable Software Features, General Purpose Simulation Packages – Arena, Extend and Others, Object Oriented Simulation, Examples of Application Oriented Simulation Packages.

UNIT III

BUILDING SIMULATION MODELS: Guidelines for Determining Levels of Model Detail, Techniques for Increasing Model Validity and Credibility,MODELING TIME DRIVEN SYSTEMS**:** Modeling Input Signals, Delays, System Integration, Linear Systems, Motion Control Models, Numerical Experimentation.

UNIT IV

EXOGENOUS SIGNALS AND EVENTS: Disturbance Signals, State Machines, Petri Nets & Analysis, System Encapsulation,MARKOV PROCESS**:** Probabilistic Systems, Discrete Time Markov Processes, Random Walks, Poisson Processes, the Exponential Distribution, Simulating a Poison Process, Continuous-Time Markov Processes.

UNIT V

EVENT DRIVEN MODELS AND SYSTEM OPTIMIZATION: Simulation Diagrams, Queuing Theory, Simulating Queuing Systems, Types of Queues, Multiple Servers,System Identification, Searches, Alpha/Beta Trackers, Multidimensional Optimization, Modeling and Simulation Mythology.

TEXT BOOKS:

1. System Modeling & Simulation, an Introduction – Frank L. Severance, John Wiley & Sons, 2001.
2. Simulation Modeling and Analysis – Averill M. Law, W. David Kelton, TMH, 3rd Edition, 2003.

REFRENCES:

1. Systems Simulation – Geoffery Gordon, PHI, 1978.

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES::RAJAMPET
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M.Tech (D E C S) I Semester
ELECTIVE I
EMBEDDED SYSTEM CONCEPTS

UNIT I

AN INTRODUCTION TO EMBEDDED SYSTEMS AND RTOS : An Embedded System, Embedded hardware units, Embedded Software in a System, , Embedded System -On-Chip (SOC) and in VLSI Circuit, Classification of Embedded systems, Architecture of kernel**,** Interrupt Servicing Mechanism, Interprocess Communication and Synchronization of Processes.

UNIT II:

PROCESSOR AND MEMORY ORGANIZATION: Structural Units In a Processor, Processor Selection for an Embedded System, Memory Devices, Memory Selection for an Embedded Systems, Allocation of Memory to Program Cache and Memory Management Links, Segments and Blocks and Memory Map of a System, DMA, Interfacing Processors, Memories and Input Output Devices.

UNIT III

DEVICES AND BUSES FOR DEVICE NETWORKS AND SOFTWARE ARCHITECTURE: CPU bus, networks for embedded systems, Computer Parallel Communication between the Networked I/O Multiple Devices using the ISA, PCI, PCI-X and Advanced Buses, Communication Interfacings: RS 232/UART, RS 422/RS 485, IEEE 488 bus, Software Architectures-Round robin, Round robin with interrupts, Function queue scheduling, RTOS.

UNIT IV

HARDWARE–SOFTWARE CO-DESIGN IN AN EMBEDDED SYSTEM: Design methodologies ,Embedded System Project Management, Embedded System Design and Co-Design Issues in System Development Process, Design Cycle in the Development Phase for an Embedded System, use of Target Systems, use of Software Tools for Development of an Embedded System, use of Scopes and Logic Analysis for System, Hardware Tests. Issues in Embedded System Design.

UNIT V

DESIGN EXAMPLES/ Case Studies: Automatic chocolate vending machine, Digital camera, Adaptive cruise control in a car, Smart cards

TEXTBOOKS:

1. Rajkamal, “Embedded systems: Architecture, Programming and Design” TMH.
2. wayne wolf, “Computers as a component: principles of embedded computing system design”.

REFERENCES:

1. Embedded system design by Arnold S Burger, CMP
2. An embedded software primer by David Simon, PEA
3. Embedded systems design:Real world design be Steve Heath; Butterworth Heinenann, Newton mass USA 2002
4. Data communication by Hayt.

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES::RAJAMPET
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M.TECH (D E C S) I SEMESTER

DIGITAL SYSTEM DESIGN LAB

a)Digital Circuit Modeling using Verilog
b) Functional verification, synthesis and implementation on FPGA

Combinational Logic:

1. Logic Gates.
2. Adders:1-bit Adders, Ripple Carry Adder, Carry Look Ahead Adder and Serial Binary Adder
3. Decoder
4. Multiplexers
5. Binary and Priority Encoders
6. Comparators

Sequential Logic:

1. Flip-Flops with Synchronous and Asynchronous inputs.
2. Counters- Ring Counter, Johnson Counter, and Up- Down Counter, Ripple Counter.
3. Shift Registers: Serial-in Serial-out, Serial in Parallel out, Parallel in Serial out and Parallel in Parallel Out.
4. Sequence Detector (Finite State Machine- Mealy and Moore Machines).
5. ALU to Perform – ADD, SUB, AND-OR, 1's and 2's COMPLIMENT, Multiplication, Division.

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES::RAJAMPET
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M.Tech (D E C S) II Semester

CODING THEORY & TECHNIQUES

UNIT I

SOURCE CODING: Mathematical model of Information, A Logarithmic Measure of Information, Entropy and Mutual Information, Source coding theorem, fixed length and variable length coding, Shannon-Fano coding, Huffman code, Huffman code applied for pair of symbols, efficiency calculations, Lempel-Ziv codes.

UNIT II

LINEAR BLOCK CODES: Introduction to Linear block codes, Matrix Description of LBC, Error Detecting and correcting capability, Encoder , Parity Check Matrix, Syndrome testing, Hamming Codes, Reed –Muller codes, Golay Codes.

UNIT III

CYCLIC CODES: Algebraic structure of cyclic codes, Binary Cyclic code properties, Encoding in systematic and non-systematic form, Encoder using (n-k) bit shift register, Syndrome Computation and Error detection, Decoding of Cyclic Codes.

UNIT IV

CONVOLUTIONAL CODES: Encoding of Convolution codes, state diagram, Tree diagram, Trellis Diagram, Optimum decoding of Convolutional code- Viterbi Algorithm,Sub Optimum Decoding of Convolutional codes-ZJ Algorithm, Fano Sequential Decoding Algorithm,Majority Logic Decoding.

UNIT V

BCH CODES: Groups, fields, binary Fields arithmetic, construction of Falois fields GF (2^m), Basic properties of Falois Fields, Computation using Falois Field GF (2^m) arithmetic, Description of BCH codes, Decoding procedure for BCH codes.

TEXT BOOKS:

1. SHU LIN and Daniel J. Costello, Jr. "Error Control Coding – Fundamentals and Applications", Prentice Hall Inc.
2. K. Sam Shanmugam, "Digital and Analog Communication Systems", Wisley Publications.

REFERENCES:

1. John G. Proakis, "Digital Communications", Mc. Graw Hill Publication.
2. Man Young Rhee, "Error Control Coding Theory", McGraw Hill Publ.
3. Symon Haykin, "Digital Communications", Wiley Publications.

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M.Tech (D E C S) II Semester

HI-SPEED NETWORKS

UNIT I

INTRODUCTION: layered architecture, Network services, High performance networks, Network elements, Basic network mechanisms, Principle and building block ISDN, ISDN protocols, Brief history of B-ISDN, principles and building block of B-ISDN, general architecture of B-ISDN, frame relay.

UNIT II

ATM NETWORKS: ATM, switching of virtual channels and virtual paths, applications of virtual channels and connections,QOS parameters, traffic descriptors, ATM service categories, ATM cell header, ATM layer, ATM adaptation layer.

UNIT III

INTERCONNECTION AND REARRANGEABLE NETWORKS: Introduction, Banyan Networks, Routing algorithm & blocking phenomenon, Batcher-Banyan networks, crossbar switch, three stage clos networks,Rearrangeable clos networks, folding algorithm, looping algorithm.

UNIT IV

ATM SIGNALING, ROUTING AND TRAFFIC CONTROL: ATM addressing, UNI signaling, PNNI signaling, PNNI routing, ABR Traffic management.

UNIT V

TCP/IP NETWORKS: History of TCP/IP, TCP application and Services, TCP, UDP, IP services and Header formats, Internetworking, TCP congestion control, Queue management: Passive & active, QOS in IP networks: differentiated and integrated services.

TEXT BOOKS:

1. William Stallings, "ISDN & B-ISDN with Frame Relay", PHI.
2. Leon Garcia widjaja, "Communication Networks", TMH, 2000.
3. N. N. Biswas, "ATM Fundamentals", Adventure books publishers, 1998.

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M.Tech (D E C S) II Semester

MICRO COMPUTER SYSTEM DESIGN

UNIT I

REVIEW OF 8086 AND 80286 PROCESSORS: Architecture, Register organization, Addressing Modes and Instruction Set (Brief treatment only), Difference between 8086 and 8088 with rest to pin structures. Architecture, Register Organization, Addressing Modes and instruction sets of 80286 (brief treatment only)

UNIT II

THE 80386, AND 80486 MICRO PROCESSORS: Architectural features, Register Organization, Memory management, Virtual 8086 mode, The Memory Paging Mechanism, Pin Definitions of 80386 and 80486 (brief treatment).

UNIT III

THE PENTIUM AND PENTIUM PRO PROCESSORS: The Memory System, Input/output system, Branch Prediction Logic, Cache Structure, Pentium Registers, Serial Pentium pro features.

THE PENTIUM IV AND DUAL CORE MICRO PROCESSORS: Architecture, Special Registers and Pin Structures (brief treatment only)

UNIT IV

I/O PROGRAMMING: Fundamentals of I/O Considerations Programmed I/O, Interrupt I/O, Block Transfers and DMA, I/O Design Example.

MULTIPROGRAMMING: Process Management, Semaphores Operations, Common Procedure Sharing, Memory Management, Virtual Memory Concept of 80286 and other advanced Processors.

UNIT V

ARITHMETIC COPROCESSOR, MMX AND SIMD TECHNOLOGIES: Data formals for Arithmetic Coprocessor, Internal Structure of 8087 and Advanced Coprocessors. Instruction Set (brief treatment).

TEXTBOOKS:

1. Barry, B. Brey, "The Intel Microprocessors,"8th Edition Pearson Education, 2009.
2. A.K. Ray and K.M. Bhurchandi,"Advanced Microprocessor and Peripherals," TMH.

REFERENCES:

1. YU-Chang, Glenn A. Gibson, "Micro Computer Systems: The 8086/8088 Family Architecture, Programming and Design" 2nd Edition, Pearson Education, 2007.
2. Douglas V. Hall, "Microprocessors and Interfacing," Special Indian Edition, 2006.

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M.Tech (D E C S) II Semester

DETECTION & ESTIMATION OF SIGNALS

UNIT I DISCRETE TIME SIGNALS : Introduction –Classification of Discrete Time Signals, Fourier Transform of Discrete time signals – Amplitude & Phase spectrum – Transfer Function – Properties of Fourier Transform.

UNIT II DETECTION THEORY - I: Introduction – Detection theory in signal processing, Detection Problem, The mathematical detection problem, Neymann-Pearson criterion, Receiver operating characteristics, Minimum Probability of error, Bayes risk criterion, Multiple Hypothesis Testing.

UNIT III DETERMINISTIC SIGNALS: Introduction, Matched Filters- Development & Performance, Generalized Matched Filters – Performance, Multiple signals, Linear Model.

UNIT IV DETECTION THEORY – II: Composite Hypothesis testing, Bayesian approach, Generalized Likelihood Ratio Test (GLRT), performance of GLRT for Large data records.

UNIT V ESTIMATION THEORY: Estimation- concepts & & Criteria, Maximum likelihood estimation, Wiener Filter for Estimation, Linear Prediction- Prediction error Process, examples- Linear Predictive vocoders, Adaptive Filters –Steepest descent Algorithm, Least Mean Square Algorithm

TEXT BOOKS:

1. Steven M. Kay, “Fundamentals of Statistical Signal Processing: Vol. 2: Detection Theory" Prentice Hall Inc., 1998(original edition) published by Pearson education 2010 India Edition.
2. Simon Haykin, “Digital Communications”, Wiley India edition, 2006.
3. James L. Melsa and David L. Cohn, “Decision and Estimation Theory," McGraw Hill, 1978.

REFERENCES:

1. Harry L. Van Trees, “Detection, Estimation and Modulation Theory, Part 1," John Wiley & Sons Inc. 1968.
2. Jerry M. Mendel, “Lessons in Estimation Theory for Signal Processing, Communication and Control," Prentice Hall Inc., 1995
3. Sophocles J. Orfanidis, “Optimum Signal Processing," 2nd edn. McGraw Hill, 1988.

Monson H. Hayes, “Statistical Digital Signal Processing and Modeling," John Wiley & Sons Inc., 1996.

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M.Tech (D E C S) II Semester

IMAGE & VIDEO PROCESSING

UNIT I

IMAGE REPRESENTATION: Importance of Image processing, Applications, Gray scale and color Images, image sampling and quantization. Two dimensional orthogonal transforms: DFT, WHT, Haar transform, KLT, DCT. Matlab: Introduction, System, GUI, Basic Image Processing Instructions.

UNIT II

IMAGE ENHANCEMENT: Filters in spatial and frequency domains, histogram-based processing – Histogram equalization (HE), Contrast Limited Adaptive Histogram Equalization, Homomorphic filtering, LOG filters, Matlab Implementation.

UNIT III

IMAGE RESTORATION: Degradation Models, PSF, circulant and block - circulant matrices, deconvolution, restoration using inverse filtering, Wiener filtering and maximum entropy-based methods, Matlab Implementation.

UNIT IV

IMAGE COMPRESSION & IMAGE SEGMENTATION: Compression models, Information theoretic perspective, Fundamental coding theorem, Lossless compression Methods, Lossy compression methods, Image compression standards.
Pixel classification, Bi-level & Multi-level Thresholding, P-tile method, Adaptive Thresholding, Edge detection, Region growing, clustering Methods-Means, Fuzzy C Means Algorithms, Matlab Implementation.

UNIT V

VIDEO PROCESSING: Representation of Digital Video, Spatio-temporal sampling, Motion Estimation, Matlab Implementation.

TEXT BOOKS:

1. R. C. Gonzalez, R. E. Woods," Digital Image Processing", Pearson Education. 2nd edition,2002
2. W. K. Pratt, "Digital image processing", Prentice Hall, 1989
3. H. C. Andrew and B. R. Hunt, "Digital image restoration", Prentice Hall, 1977
4. A. M. Tekalp, "Digital Video Processing", Prentice-Hall, 1995
5. A. Bovik, "Handbook of Image & Video Processing", Academic Press, 2000

REFERENCES:

1 R. Jain, R. Kasturi and B.G. Schunck, "Machine Vision", McGraw-Hill International Edition, 1995.

2 Dr.M.N.GiriPrasad et. al "*Feature Extraction from Micrograph Images Using Watershed Segmentation Approach*", International Journal of Applied Engineering Research, vol.5, Number 23-24(2010), pp.3665-3674, 2010.(ISSN 0973 - 4562)

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M.Tech (D E C S) II Semester

DSP PROCESSORS & ARCHITECTURES
ELECTIVE - II

UNIT I

INTRODUCTION TO DIGITAL SIGNAL PROCESING: Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS: Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT II

ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT III

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS: Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

UNIT IV

IMPLEMENTATIONS OF BASIC DSP ALGORITHMS: The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

IMPLEMENTATION OF FFT ALGORITHMS: An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

UNIT V

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES: Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS:

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. DSP Processor Fundamentals, Architectures & Features – Lapsley et al.S. Chand & Co, 2000.

REFERENCES:

1. Digital Signal Processors, Architecture, Programming and Applications-B.Venkata Ramani and M. Bhaskar, TMH, 2004.
2. Digital Signal Processing – Jonatham Stein, John Wiley, 2005.

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES::RAJAMPET
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M.Tech (D E C S) II Semester

NEURAL NETWORKS & APPLICATIONS
ELECTIVE - II

UNIT I

INTRODUCTION: History of Neural Networks, Structure and functions of biological and artificial neuron, Neural network architectures, learning methods, evaluation of neural networks.

UNIT II

SUPERVISED LEARNING: McCulloch- Pitts neuron model, perception learning, Delta learning, Windrow- Hoff learning rules, linear seperability, Adeline modification.

MULTI LAYER NETWORKS: Architectures, Madalines, Back propagation algorithm, importance of learning parameter and momentum term, radial basis functions, polynomial networks.

UNIT III

UNSUPERVISED LEARNING : Winner-Take- all learning, out star learning, learning vector quantizers, Counter propagation networks, Kohonen self – organizing networks, Grossberg layer, adaptive resonance theory, Hamming net.

UNIT IV

ASSOCIATIVE MEMORIES: Hebbian learning rule, continues and discrete Hopfild networks, recurrent and associative memory, Boltzman machines, Bi-directional associative memory.

UNIT V

APPLICATIONS OF NEURAL NETWORKS: Optimization, Travelling Salesman problem, solving simultaneous linear equations, application in pattern recognition and image processing. Pattern recognition, Optimization, Associative memories, speech and decision-making. VLSI implementation of neural networks.

TEXT BOOKS:

1. J.M. Zurada, “Introduction to Artificial Neural Systems” - Jaico Publishing House, Bombay,2001.
2. Kishan Mehrotra , Chelkuri. K.Mohan, Sanjay Ranka, “Elements of Artificial Neural Networks”, Penram International
3. B.Yagnanarayana, “Artificial Neural Networks”, PHI, New Delhi.

REFERENCES:

1. S.N Sivanandham, S. sumathi, S.N.Deepa,“Introduction to Neural networks using matlab 6.0”, Tata McGraw Hill, New Delhi, 2005.
2. P.D. wasserman, “Neural computing theory & practice”, ANZA PUB.

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M.Tech (D E C S) II Semester

COMPRESSION TECHNIQUES
ELECTIVE - II

UNIT I

REVIEW OF INFORMATION THEORY: The discrete memory less information source, Kraft inequality; optimal codes Source coding theorem. Compression Techniques, Lossless and Lossy Compression, Mathematical Preliminaries for Lossless Compression, Huffman Coding, Optimality of Huffman codes, Extended Huffman Coding, Adaptive Huffman Coding, Arithmetic Coding, Adaptive Arithmetic coding, Run Length Coding.

UNIT II

DICTIONARY TECHNIQUES: Static Dictionary, Adaptive Dictionary, LZ77, LZ78, LZW, Applications, Predictive Coding, Prediction with Partial Match, Burrows Wheeler Transform, Sequitur, Lossless Compression Standards (files, text, and images, faxes), Dynamic Markov Compression.

UNIT III

MATHEMATICAL PRELIMINARIES FOR LOSSY CODING: Rate distortion theory: Rate distortion function R(D),Properties of R(D); Calculation of R(D) for the binary source and the Gaussian source, Rate distortion theorem, Converse of the Rate distortion theorem,

UNIT IV

QUANTIZATION AND MATHEMATICAL PRELIMINARIES FOR TRANSFORMS: Uniform & Non-uniform, optimal and adaptive quantization, vector quantization and structures for VQ, Optimality conditions for VQ, Predictive Coding, Differential Encoding Schemes, Karhunen Loeve Transform, Discrete Cosine and Sine Transforms, Discrete Walsh Hadamard Transform, Lapped transforms- Transform coding, Subband coding, Wavelet Based Compression, Analysis/Synthesis Schemes.

UNIT V

DATA AND IMAGE COMPRESSION STANDARDS: Zip and Gzip, Speech Compression Standards: MPEG, JPEG 2000. MPEG, H264, Binary Image Compression Standards, Continuous Tone Still Image Compression Standards, Video Compression Standards.

TEXT BOOKS:

1. Khalid Sayood, “Introduction to Data Compression”, Morgan Kaufmann Publishers., Second Edn., 2005.
2. David Salomon, “Data Compression: The Complete Reference”, Springer Publications, 4th Edn., 2006.
3. Thomas M. Cover, Joy A. Thomas, “Elements of Information Theory," John Wiley & Sons, Inc.,1991.

REFERENCES:

1. Toby Berger, “Rate Distortion Theory: A Mathematical Basis for Data Compression”, Prentice Hall, Inc., 1971.
2. K.R.Rao, P.C.Yip, “The Transform and Data Compression Handbook”, CRC Press., 2001.
3. R.G.Gallager, “Information Theory and Reliable Communication”, John Wiley & Sons, Inc., 1968

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M.Tech (D E C S) II Semester

ADVANCED COMMUNICATIONS LABORATORY

1. To simulate a basic Quaternary Phase Shift Keying (QPSK)
2. To evaluate Rayleigh and Rician multipath fading channel
3. Decision Feedback Equalization using RLS algorithm
4. Generation of Basic Waveforms (signals & Sequences).
5. Designs of Low pass FIR Filter using any two windowing techniques.
6. Comparative Analysis of Windowing Techniques using GUI tools.
7. Design Butterworth analog filters.
8. Design Chebyshev low pass filter.
9. Gray scale Image Enhancement using Contrast Enhancement Techniques
10. Color Image Enhancement using Contrast Enhancement Techniques
11. Denoising the images using Average and Median Filters.
12. Deblurring Images using a Weiner Filter.
13. Comparison of Image edge detection methods.
14. Morphological Image Processing Operations.
15. Conversion of a multiframe image to a movie.

Note: Use MATLAB 7.8.0 (R2009a) and above