ACADEMIC REGULATIONS

Applicable for students admitted into M.Tech. Programme from 2017-18

The Jawaharlal Nehru Technological University Anantapur shall confer M.Tech. Post graduate degree to candidates who are admitted to the Master of Technology Programmes and fulfill all the requirements for the award of the degree.

1. ELIGIBILITY FOR ADMISSIONS:

Admission to the above programme shall be made subject to the eligibility, qualifications and specialization prescribed by the competent authority for each programme, from time to time.

Admissions shall be made either on the basis of merit rank obtained by the qualifying candidates at an Entrance Test conducted by the University or on the basis of GATE/PGECET score, subject to reservations or policies framed by the Government of Andhra Pradesh policies from time to time.

2. ADMISSION PROCEDURE:

As per the existing stipulations of AP State Council for Higher Education (APSCHE), Government of Andhra Pradesh, admissions are made into the first year as follows

a) Category-A seats are to be filled by Convenor through PGECET/GATE score.

b) Category-B seats are to be filled by Management as per the norms stipulated by Government of A. P.

3. SPECIALIZATION:

The following specializations are offered at present for the M.Tech. Programme.

Sl. No.	**Specialization**
1.	CAD/CAM
2	Machine Design
2.	Digital Electronics and Communication Systems
3.	Embedded Systems
4.	VLSI System Design
5.	Computer Science and Engineering
6.	Electrical Power Engineering
7.	Electrical Power Systems
8	Structural Engineering

and any other specialization as approved by the concerned authorities from time to time.

4. COURSE WORK:

4.1. A Candidate after securing admission must pursue the M. Tech. programme of study for four semesters duration.

4.2. Each semester shall be of 20 weeks duration including all examinations.

4.3. A candidate admitted in to the programme should complete it within a period equal to twice the prescribed duration of the programme from the date of admission.

5. ATTENDANCE

5.1. A candidate shall be deemed to have eligibility to write end semester examinations if he has put in at least 75% of attendance aggregate in all subjects/courses in the semester.

5.2. Condonation of shortage of attendance up to 10% i.e., between 65% and above and less than 75% may be granted by the Institute Academic committee.

5.3. Shortage of attendance below 65% in aggregate shall in no case be condoned.

5.4. Condonation of shortage of attendance shall be granted only on genuine and valid reasons on representation by the candidate with supporting evidence.

5.5. A stipulated fee shall be payable towards condonation of shortage of attendance to the institute as per following slab system

1st Slab: Less than 75% attendance but equal to or greater than 70% a normal condonation fee can be collected from the student.

2nd Slab: Less than 70% but equal to or greater than 65%, double the condonation fee can be collected from the student.

5.6. Students whose shortage of attendance is not condoned in any semester are not eligible to take their end examination of that class and their registration shall stand cancelled for that semester.

5.7. A student will not be promoted to the next semester unless he satisfies the attendance requirements of the current semester, as applicable.

5.8. A student detained due to shortage of attendance, will have to repeat that semester when offered next.

6. CREDIT SYSTEM NORMS:

TABLE 1

	Period(s)/week	**Credits**
Theory	01	01
Practical	03	02
Seminar	01	01
Project	-	16

7. EVALUATION:

7.1 Distribution of marks

S. No	Examination	Marks	Examination and Evaluation	Scheme of Evaluation
1.	Theory	60	Semester-end examination (External evaluation)	The question paper shall be of descriptive type with 5 questions with internal choice are to be answered in 3hours duration of the examination.
		40	Mid - Examination of 120 Min. duration (Internal evaluation). 4 descriptive type questions with internal choice are to be answered and evaluated for 30 marks, and the reaming 10 marks are to be allotted for 3-5 assignments to be submitted by the student. The assignment marks are to be awarded based on the completeness of the assignment, correctness of the assignment and in-time submission, evaluated for 10 marks and average of the total assignment marks are rounded to the next integer.	Two mid-exams 30 marks each are to be conducted. Better one to be considered. **Mid-I:** After first spell of instructions (I&II Units). **Mid-II:** After second spell of instructions (III - V Units).
2	Laboratory	60	Semester-end Lab Examination (External evaluation)	**For laboratory courses: 3** hours duration. One External and One Internal examiners.

S. No	Examination	Marks	Examination and Evaluation		Scheme of Evaluation
		40	30	Day to Day evaluation (Internal evaluation)	Performance in laboratory experiments.
			10	Internal evaluation	Practical Tests (one best out of two tests includes viva-voce)
3	Seminar in each of the semesters. 2 hours /week	100	Internal Evaluation 20 Marks for Report 20 Marks for subject content 40 Marks for presentation 20 Marks for Question and Answers		Continuous evaluation during a semester by the Departmental Committee (DC)
4	Project work	Grade A (95%) Grade B (85%)	12 credits	External evaluation	End Project Viva-Voce Examination by Committee as detailed under sect. 9.
			4 credits	Internal evaluation	Continuous evaluation by the DC. as detailed under sect. 9.5

7.2 A candidate shall be deemed to have secured the minimum academic requirement in a subject/practical if he secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

7.3 A candidate has to secure a minimum of 50% to be declared successful.

7.4 In case the candidate does not secure the minimum academic requirement in any of the subjects/practical, he has to reappear for the Examination either supplementary or regular in that subject/practical along with the next batch students. A separate supplementary examinations will be conducted for the I semester students at the end of II semester.

7.5 **Revaluation / Recounting:** Students shall be permitted to request for recounting/ revaluation of the end theory examination answer

scripts within a stipulated period after payment of prescribed fee. After recounting or revaluation, records are updated with changes if any and the student will be issued a revised memorandum of marks. If there are no changes, the student shall be intimated the same through a letter or a notice.

8. RE-REGISTRATION FOR IMPROVEMENT OF INTERNAL EVALUATION MARKS(for theory subjects only):

8.1 Out of the subjects the candidate has failed in the examination due to internal evaluation marks secured being less than 50%, the candidate shall be given one chance for each theory subject and for a maximum of **Three** theory subjects for improvement of internal evaluation marks.

8.2 The candidate can re-register for the chosen subjects and fulfill the academic requirements. Re-registration shall not be permitted after the commencement of class work for that semester. The candidate can re-register for 1st semester subjects when he is in his 3rd semester and for 2nd semester subjects when he is in his 4th semester else the candidate can re-register after completion of 2 years course work.

8.3 For each subject re-registered, the candidate has to pay a fee equivalent to one third of the semester tuition fee.

8.4 In the event of re-registration, the internal evaluation marks as well as the End Examinations marks secured in the previous attempt(s) for those subjects stand cancelled.

9. EVALUATION OF PROJECT WORK:

Every candidate shall be required to submit thesis/dissertation after taking up a topic approved by the Departmental Committee.

9.1 The Departmental Committee (DC) consisting of HOD, Project supervisor and two internal senior experts shall monitor the progress of the project work. A Project Review Committee (PRC) shall be constituted with Principal as Chair Person, Heads of the departments of the M.Tech Programs and Two other senior faculty members, as members of the PRC. PRC will come into action when the DC is not able to resolve the issues.

9.2 Registration of Project work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the courses (theory, practical and seminar of I & II semesters).

9.3 After satisfying 9.2, a candidate has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work to the DC for approval. Only after obtaining the approval of DC, the student can initiate the project work.

9.4 The work on the project shall be initiated in the penultimate semester and continued in the final semester. The duration of the project is for two semesters. The candidate can submit Project thesis with the approval of DC after 36 weeks from the date of registration at the earliest but not later than one calendar year from the date of registration for the project work. Extension of time within the total permissible limit for completing the programme is to be obtained from the Head of the Institution.

9.5 The Internal Evaluation shall be made by the DC to grade, on the basis of two seminars presented by the student on the topic of his project.

9.6 The student must submit status report at least in two different phases during the project work period. These reports must be approved by the DC before submission of the Project Report.

9.7 A candidate shall be allowed to submit the thesis / dissertation only after passing all the prescribed subjects (theory, practical, seminar and project work internal evaluation).

9.8 A candidate has to prepare four copies of the thesis/dissertation certified in the prescribed format by the supervisor and HOD. Out of which three copies shall be submitted in the examination section.

9.9 Viva-voce examination shall be conducted by a board consisting of the supervisor, Head of the department and the examiner. The board shall jointly report candidate's work as.

A Very Good performance
B Moderate Performance
C Failure Performance

Head of the Department shall coordinate and make arrangements for the conduct of viva-voce.

If the report of the viva-voce is failure performance, the candidate will retake the viva-voce examination after three months. If he fails to get a satisfactory report at the second viva-voce examination, he will not be eligible for the award of the degree.

10. CREDIT POINT AVERAGE AND CUMULATIVE CREDIT POINT AVERAGE:

10.1. CREDIT POINT AVERAGE (CPA):

$$\mathbf{CPA} = \frac{\sum_i C_i T_i}{10 \sum_i C_i}$$

Where C_i= Credits earned for Course i in any semester/year.

T_i= Total marks obtained for course i in any semester/year.

10.2. CUMULATIVE CREDIT POINT AVERAGE (CCPA):

$$\textbf{CCPA} = \frac{\sum_n \sum_i C_{ni} T_{ni}}{10 \sum_n \sum_i C_{ni}}$$

Where ***n*** refers to the semester in which such courses were credited.

The CCPA is awarded only when a student earns all the credits prescribed for the programme.

10.3. OVERALL PERFORMANCE:

CCPA	Classification of Final Results
7.0 and above	First Class with Distinction
6.0 and above but below 7.0	First Class
5.0 and above but below 6.0	Second Class

11. TRANSCRIPTS:

After successful completion of the entire programme of study, a transcript containing performance of all the academic years will be issued as a final record. Duplicate transcripts will be issued if required, after payment of requisite fee. Partial transcript will also be issued up to any point of study to a student on request.

12. ELIGIBILITY:

A student shall be eligible for the award of M.Tech Degree if he fulfills all the following conditions:

i. Registered and successfully completed all the components prescribed in the programme of study to which he was admitted.
ii. Successfully acquired all **72 credits** as specified in the curriculum corresponding to the branch of his study within the stipulated time.
iii. No disciplinary action is pending against him.

13. AWARD OF DEGREE:

The Degree will be conferred and awarded by Jawaharlal Nehru Technological University Anantapur, Anantapur on the recommendations of the Principal, AITS (Autonomous) based on the eligibility as mentioned in clause 11.

14. WITHHOLDING OF RESULTS:

If the candidate has any dues to the Institute or if any case of in-discipline is pending against him, the result of the candidate shall be withheld and he will not be allowed / promoted into the next higher semester. The issue of degree is liable to be withheld in such cases.

15. TRANSITORY REGULATIONS:

Candidates who have discontinued or have been detained for want of attendance or who have failed after having undergone the course in earlier regulations and

wish to continue the course are eligible for admission into the unfinished semester from the date of commencement of class work with the same or equivalent subjects as and when subjects are offered. Whereas, he continues to be in the academic regulations he was first admitted.

16. AMENDMENTS OF REGULATIONS:

The Chairman, Academic Council of Annamacharya Institute of Technology and Sciences, Rajampet (Autonomous) reserves the right to revise, amend, or change the Regulations, Scheme of Examinations and/or Syllabi or any other policy relevant to the needs of the society or industrial requirements etc., without prior notice.

17. GENERAL:

Where the words "he", "him", "his", occur in the regulations, they include "she", "her", "hers".

18. Any legal issues are to be resolved in Rajampet Jurisdiction.

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Annamacharya Institute of Technology and Sciences, Rajampet.	
Curriculum for the Programmes under Autonomous Scheme	
Regulation	R 2017
Department	Department of Electronics and Communication Engineering
Programme Code & Name	PC: M.Tech. VLSI System Design
Semester I	

Course Code	Course Name	Hours/ Week		Credit	Maximum marks		
		L	P	C	Internal	External	Total
7PC311	VLSI Technology	4	0	4	40	60	100
7PC312	Analog IC Design	4	0	4	40	60	100
7PC313	Digital IC Design	4	0	4	40	60	100
7PC314	Modelling and synthesis through Verilog HDL	4	0	4	40	60	100
7PC315	FPGA Architectures and Applications	4	0	4	40	60	100
	Elective – I	4	0	4	40	60	100
7PC316	Seminar – I	0	0	2	100	00	100
7PC317	VLSI Design Lab-I	0	3	2	40	60	100
Total		24	3	28	800		
Semester II							
Course Code	Course Name	Hours/ Week		Credit	Maximum marks		
		L	P	C	Internal	External	Total
7PB321	Testing and Testability	4	0	4	40	60	100
7PC321	Low Power VLSI Design	4	0	4	40	60	100
7PB323	Hardware Software Co-Design	4	0	4	40	60	100
7PC322	ASIC Design	4	0	4	40	60	100
7PC323	Algorithms for VLSI Design Automation	4	0	4	40	60	100
	Elective – II	4	0	4	40	60	100
7PC326	Seminar – II	0	0	2	100	00	100
7PC327	VLSI Design Lab- II	0	3	2	40	60	100
Total		24	3	28	800		
Semester III & IV							
Course Code	Course Name	Credit		Maximum Marks			
		C		Internal	External		Total
7PC331	**PROJECT**	**16**		**GRADE(A/B/C)**			

List of Electives		
Elective – I	7PB311	Embedded System Concepts
	7PA315	System Modeling and Simulation
	7PC318	Scripting Languages for VLSI Design Automation
Elective – II	7PC324	Nano Electronics
	7PC325	VLSI Signal Processing
	7PB324	DSP Processors and Architectures

ANNAMACHARYA INSTITUTE OF TECHNOLOGY AND SCIENCES, RAJAMPET
(AN AUTONOMOUS INSTITUTION)
M.Tech (VLSI SYSTEM DESIGN) I Semester

VLSI TECHNOLOGY

UNIT I
REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGIES: (MOS, CMOS, Bi-CMOS) Technology Trends and Projections.

Ids -Vds Relationships, Threshold Voltage V_t, G_m, G_{ds} and W_o, Pass Transistor, MOS,CMOS & Bi- CMOS Inverters, Zpu/Zpd, MOS Transistor Circuit Model, Latch-Up in CMOS Circuits.

UNIT II

LAYOUT DESIGN AND TOOLS: Transistor Structures, Wires and Vias, Scalable Design Rules, Layout Design Tools.

UNIT III

LOGIC GATES & LAYOUTS: Static Complementary Gates, Switch Logic, Alternative Gate Circuits, Low Power Gates, Resistive and Inductive Interconnect Delays.

UNITIV

COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network delay, Interconnect Design, Power Optimization, Switch Logic Networks, Gate and Network Testing.

UNIT V

SEQUENTIAL SYSTEMS: Memory Cells and Arrays, Clocking Disciplines, Design, Power Optimization, Design Validation and Testing.

FLOOR PLANNING & ARCHITECTURE DESIGN: Floor Planning Methods, Off-Chip Connections, High Level Synthesis, Architecture for Low Power, SOCs and Embedded CPUs, Architecture Testing.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian et . al(3 authors) PHI of India Ltd.,2005
2. Modern VLSI Design, 3rd Edition, Wayne Wolf , Pearson Education, fifth Indian Reprint, 2005.

REFERENCES:

1. Principals of CMOS Design – N.H.E Weste, K.Eshraghian, Adison Wesley, 2nd Edition.
2. Introduction to VLSI Design – Fabricius, MGH International Edition, 1990.
3. CMOS Circuit Design, Layout and Simulation – Baker, Li Boyce, PHI, 2004.

ANNAMACHARYA INSTITUTE OF TECHNOLOGY AND SCIENCES, RAJAMPET
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M.Tech (VLSI SYSTEM DESIGN) I Semester

ANALOG IC DESIGN

UNIT I

INTEGRATED DEVICES AND MODELING AND CURRENT MIRROR: Advanced MOS Modeling, Large Signal and Small Signal Modeling for BJT/Basic Current Mirrors and Single Stage Amplifiers: Simple CMOS Current Mirror, Common Source, Common Gate Amplifier With Current Mirror Active Load. Source Follower with Current Mirror to Supply Bias Current, High Output Impedance Current Mirrors and Bipolar Gain Stages. Frequency Response.

UNIT II

OPERATIONAL AMPLIFIER DESIGN AND COMPENSATION: Two Stage CMOS Operational Amplifier. Feedback and Operational Amplifier Compensation. Advanced Current Mirror. Folded–Cascade Operational Amplifier, Current Mirror Operational Amplifier Fully Differential Operational Amplifier. Common Mode Feedback Circuits. Current Feedback Operational Amplifier. Comparator . Charge Injection Error. Latched Comparator and Bi-CMOS Comparators.

UNIT III

SAMPLE AND HOLD SWITCHED CAPACITOR CIRCUITS: MOS, CMOS, Bi-CMOS Sample and Hold Circuits. Switched Capacitor Circuits: Basic Operation and Analysis. First Order and Biquard Filters. Charge Injection. Switched Capacitor Gain Circuit. Correlated. Double Sampling Techniques. Other Switched Capacitor Circuits.

UNIT IV

DATA CONVERTERS: Ideal D/A & A/D Converters. Quantization Noise. Performance Limitations. Nyquist Rate D/A Converters: Decoders Based Converters. Binary Scaled Converters. Hybrid Converters. Nyquist Rate A/D Converters: Integrating ,Successive Approximation, Cyclic Flash Type, Two Step, Interpolating, Folding and Pipelined, A/D Converters.

UNIT V

OVER SAMPLING CONVERTERS AND FILTERS: Over Sampling With and Without Noise Shaping .Digital Decimation Filter. High Order Modulators. Band Pass Over Sampling Converter. Practical Considerations. Continuous Time Filters.

TEXT BOOKS:

1. D.A.JOHN & KEN MARTIN: “Analog Integrated Circuit Design”. John Wiley, 1997.
2. Behzad Razavi, “Design of Analog CMOS Integrated Circuit” Tata-Mc GrawHill, 2002

REFERENCES:

1. Philip Allen & Douglas Holberg, “CMOS Analog Circuit Design”, Oxford University Press, 2002
2. GREGOLIAN &TEMES: Analog MOS Integrated Circuits, John Wiley, 1986.

ANNAMACHARYA INSTITUTE OF TECHNOLOGY AND SCIENCES, RAJAMPET
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M.Tech (VLSI SYSTEM DESIGN) I Semester

DIGITAL IC DESIGN

UNIT I

CMOS inverters -static and dynamic characteristics.

UNIT II
Static and Dynamic CMOS design- Domino and NORA logic - combinational and sequential circuits.

UNIT III
Method of Logical Effort for transistor sizing -power consumption in CMOS gates- Low power CMOS design.

UNIT IV
LAYOUT DESIGN RULES: Need for Design Rules, NMOS and CMOS Based Design Rules, Simple Layout Examples, Sheet Resistance, Area Capacitance, Wiring Capacitances , Drive Large Capacitive Load**.**

UNIT V
SUBSYSTEM DESIGN PROCESS: Arithmetic circuits in CMOS VLSI - Adders- multipliers- shifter -CMOS memory design - SRAM and DRAM, modified Booth's algorithm for multipliers, Design of ALU subsystem , Implementing ALU functions with an adder.

TEXT BOOKS:

1. Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits - Analysis & Design", MGH, Second Ed., 1999
2. Jan M Rabaey, "Digital Integrated Circuits - A Design Perspective", Prentice Hall, 1997
3. Eugene D Fabricus, "Introduction to VLSI Design,"McGraw Hill International Edition.1990

REFERENCES:

1. Ken Martin, "Digital Integrated Circuit Design", Oxford University Press, 2000
2. Neil H E West and Kamran Eshranghian,"Principles of CMOS VLSI Design: A System Perspective", Addision-Wesley 2nd Edition,2002.

ANNAMACHARYA INSTITUTE OF TECHNOLOGY AND SCIENCES, RAJAMPET
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M.Tech (VLSI SYSTEM DESIGN) I Semester

MODELLING AND SYNTHESIS THROUGH VERILOG HDL

UNIT I

HARDWARE MODELING WITH THE VERILOG HDL : Hardware Encapsulation -The Verilog Module, Hardware Modeling Verilog Primitives, Descriptive Styles, Structural Connections, Behavioral Description In Verilog, Hierarchical Descriptions of Hardware, Structured (Top Down) Design Methodology, Arrays of Instances, Using Verilog for Synthesis, Language Conventions, Representation of Numbers, Verilog Variables, Logic Value Set, Data Types, Strings, Constants, Operators, Expressions and Operands, Operator Precedence.

UNIT II

LOGIC SYSTEM MODELING IN VERILOG HDL: User-Defined Primitives, User Defined Primitives – Combinational Behavior User-Defined Primitives –Sequential Behavior, Initialization of Sequential Primitives. Models Of Propagation Delay; Built-In Constructs for Delay, Signal Transitions, Verilog Models for Gate Propagation Delay (Inertial Delay), Time Scales for Simulation, Verilog Models for Net Delay (Transport Delay), Module Paths and Delays, Path Delays and Simulation, Inertial Delay Effects and Pulse Rejection.

UNIT III

SWITCH-LEVEL MODELS IN VERILOG:MOS Transistor Technology, Switch Level Models of MOS Transistors, Switch Level Models of Static CMOS Circuits, Alternative Loads and Pull Gates, CMOS Transmission Gates. Bio-Directional Gates (Switches), Signal Strengths, Ambiguous Signals, Strength Reduction By Primitives, Combination and Resolution of Signal Strengths, Signal Strengths and Wired Logic.

BEHAVIORAL DESCRIPTIONS IN VERILOG HDL: Verilog Behaviors, Behavioral Statements, Procedural Assignment, Procedural Continuous Assignments, Procedural Timing Controls and Synchronization, Intra-Assignment, Delay-Blocked Assignments, Non-Blocking Assignment, Intra-Assignment Delay: Non-Blocking Assignment, Simulation of Simultaneous Procedural Assignments, Repeated Intra Assignment Delay, Indeterminate Assignments and Ambiguity, Constructs for Activity Flow Control, Tasks and Functions, Summary of Delay Constructs in Verilog, System Tasks for Timing Checks, Variable Scope Revisited, Module Contents, Behavioral Models of Finite State Machines.

UNIT IV

SYNTHESIS OF COMBINATIONAL AND SEQUENTIAL LOGIC: HDL-Based Synthesis, Technology-Independent Design, Benefits of Synthesis, Synthesis Methodology, Vendor Support, Styles for Synthesis of Combinational Logic, Technology Mapping and Shared Resources, Three State Buffers, Three State Outputs and Don't Cares.

Synthesis of Sequential Logic Synthesis of Sequential Udps, Synthesis of Latches, Synthesis of Edge-Triggered Flip Flops, Registered Combinational Logic, Shift Registers and Counters, Synthesis of Finite State Machines, Resets, Synthesis of Gated Clocks, Design Partitions and Hierarchical Structures.

UNIT V

SYNTHESIS OF LANGUAGE CONSTRUCTS: Synthesis of Nets, Synthesis of Register Variables, Restrictions on Synthesis of "X" and "Z", Synthesis of Expressions and Operators, Synthesis of Assignments, Synthesis of Case and Conditional Statement, Synthesis of Resets, Timings Controls in Synthesis, Synthesis of Multi-Cycle Operations, Synthesis of Loops, Synthesis if Fork Join Blocks, Synthesis of The Disable Statement Synthesis of User-Defined

Tasks, Synthesis of User-Defined Functions, Synthesis of Specify Blocks, Synthesis of Compiler Directives.

TEXT BOOKS:

a. M.D.CILETTI, "Modeling, Synthesis and Rapid Prototyping with the Verilog HDL", Prentice-Hall, 1999.
b. Samir Palanitkar, "Verilog HDL" Pearson Education, 2002.

REFERENCES:

1. M.G.ARNOLD, "Verilog Digital – Computer Design", Prentice-Hall (PTR), 1999.

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ANNAMACHARYA INSTITUTE OF TECHNOLOGY AND SCIENCES, RAJAMPET
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M.Tech (VLSI SYSTEM DESIGN) I Semester

FPGA ARCHITECTURE & APPLICATIONS

UNIT I

PROGRAMMABLE LOGIC: ROM, PLA, PAL, PLD, PGA – Features, Programming and Applications using Complex Programmable Logic Devices Altera Series – Max 5000/7000 Series and Altera FLEX Logic – 10000 Series CPLD, AMD's – CPLD (Mach 1 To 5); Cypres FLASH 370 Device Technology, Lattice Plsi's Architectures – 3000 Series – Speed Performance and in System Programmability.

UNIT II

FPGA: Field Programmable Gate Arrays – Programming technologies, Logic Blocks, Routing Architecture, Design Flow, Technology Mapping for Fpgas.

UNIT III

COMMERCIAL FPGA'S: Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT & T – ORCA's (Optimized Reconfigurable Cell Array): ACTEL's – ACT-1,2,3 and Their Speed Performance.

UNIT IV

REALIZATION OF STATE MACHINE: Top Down Design – State Transition Table, State Assignments for FPGAs. Problem of Initial State Assignment for One Hot Encoding. Charts with a PAL. Alternative Realization for State Machine Chart using Microprogramming. Linked State Machines. One – Hot State Machine, Petrinetes for State Machines – Basic Concepts, Properties. Extended Petrinetes for Parallel Controllers. Finite State Machine – Ex: Traffic Light Controller, Implementation of Petrinet Description

UNIT V

FSM ARCHITECTURES AND SYSTEMS LEVEL DESIGN: Architectures Centered Around Non-Registered PLDs. State Machine Designs Centered Around Shift Registers. One – Hot Design Method. Use of ASMs in One – Hot Design. Application of One – Hot Method. System Level Design – Controller, Data Path and Functional Partition.

TEXT BOOKS/ REFERENCES:

1. P.K.Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, jPrentice Hall (Pte), 1994.
2. S.Trimberger, Edr., Field Programmable Gate Array Technology, Kluwer Academic Publicatgions,1994.
3. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley & Sons, Newyork, 1995.
4. S.Brown, R.Francis, J.Rose, Z.Vransic, Field Programmable Gate Array, Kluwer Pubin, 1992.
5. Richard F. Tinder, Engineering Digital Design, Second Edition, Academic Press.

M.Tech (VLSI SYSTEM DESIGN) I Semester

ELECTIVE I
EMBEDDED SYSTEM CONCEPTS

UNIT I

AN INTRODUCTION TO EMBEDDED SYSTEMS AND RTOS : An Embedded System, Embedded hardware units, Embedded Software in a System, , Embedded System -On-Chip (SOC) and in VLSI Circuit, Classification of Embedded systems, Architecture of kernel**,** Interrupt Servicing Mechanism, Interprocess Communication and Synchronization of Processes.

UNIT II:

PROCESSOR AND MEMORY ORGANIZATION: Structural Units In a Processor, Processor Selection for an Embedded System, Memory Devices, Memory Selection for an Embedded Systems, Allocation of Memory to Program Cache and Memory Management Links, Segments and Blocks and Memory Map of a System, DMA, Interfacing Processors, Memories and Input Output Devices.

UNIT III

DEVICES AND BUSES FOR DEVICE NETWORKS AND SOFTWARE ARCHITECTURE: CPU bus, networks for embedded systems, Computer Parallel Communication between the Networked I/O Multiple Devices using the ISA, PCI, PCI-X and Advanced Buses, Communication Interfacings: RS 232/UART, RS 422/RS 485, IEEE 488 bus, Software Architectures-Round robin, Round robin with interrupts, Function queue scheduling, RTOS.

UNIT IV

HARDWARE–SOFTWARE CO-DESIGN IN AN EMBEDDED SYSTEM: Design methodologies ,Embedded System Project Management, Embedded System Design and Co-Design Issues in System Development Process, Design Cycle in the Development Phase for an Embedded System, use of Target Systems, use of Software Tools for Development of an Embedded System, use of Scopes and Logic Analysis for System, Hardware Tests. Issues in Embedded System Design.

UNIT V

DESIGN EXAMPLES/ Case Studies: Automatic chocolate vending machine, Digital camera, Adaptive cruise control in a car, Smart cards

TEXTBOOKS:

1. Rajkamal, “Embedded systems: Architecture, Programming and Design” TMH.
2. wayne wolf, “Computers as a component: principles of embedded computing system design”.

REFERENCES:

1. Embedded system design by Arnold S Burger, CMP
2. An embedded software primer by David Simon, PEA
3. Embedded systems design:Real world design be Steve Heath; Butterworth Heinenann, Newton mass USA 2002
4. Data communication by Hayt.

ANNAMACHARYA INSTITUTE OF TECHNOLOGY AND SCIENCES, RAJAMPET
(AN AUTONOMOUS INSTITUTION)
M.Tech (VLSI SYSTEM DESIGN) I Semester

ELECTIVE I
SYSTEM MODELLING & SIMULATION

UNIT I

Basic Simulation Modeling, Systems, Models and Simulation, Discrete Event Simulation, Simulation of Single Server Queuing System, Simulation of Inventory System, Alternative approach to Modeling and Simulation.

UNIT II

SIMULATION SOFTWARE: Comparison of Simulation Packages with Programming Languages, Classification of Software, Desirable Software Features, General Purpose Simulation Packages – Arena, Extend and Others, Object Oriented Simulation, Examples of Application Oriented Simulation Packages.

UNIT III

BUILDING SIMULATION MODELS: Guidelines for Determining Levels of Model Detail, Techniques for Increasing Model Validity and Credibility,MODELING TIME DRIVEN SYSTEMS**:** Modeling Input Signals, Delays, System Integration, Linear Systems, Motion Control Models, Numerical Experimentation.

UNIT IV

EXOGENOUS SIGNALS AND EVENTS: Disturbance Signals, State Machines, Petri Nets & Analysis, System Encapsulation,MARKOV PROCESS**:** Probabilistic Systems, Discrete Time Markov Processes, Random Walks, Poisson Processes, the Exponential Distribution, Simulating a Poison Process, Continuous-Time Markov Processes.

UNIT V

EVENT DRIVEN MODELS AND SYSTEM OPTIMIZATION: Simulation Diagrams, Queuing Theory, Simulating Queuing Systems, Types of Queues, Multiple Servers,System Identification, Searches, Alpha/Beta Trackers, Multidimensional Optimization, Modeling and Simulation Mythology.

TEXT BOOKS:

1. System Modeling & Simulation, an Introduction – Frank L. Severance, John Wiley & Sons, 2001.
2. Simulation Modeling and Analysis – Averill M. Law, W. David Kelton, TMH, 3rd Edition, 2003.

REFRENCES:

1. Systems Simulation – Geoffery Gordon, PHI, 1978

ELECTIVE I
SCRIPTING LANGUAGE FOR VLSI DESIGN AUTOMATION

UNIT I
Overview of Scripting Languages – PERL, CGI, VB Script, Java Script.

UNIT II
PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables.

UNIT III
Inter process Communication Threads, Compilation & Line Interfacing.

UNIT IV
Debugger Internal & Externals Portable Functions. Extensive Exercises for Programming in PERL .

UNIT V
Other Languages: Broad Details of CGI, VB Script, Java Script with Programming Examples.

TEXT BOOKS:

1. Randal L, Schwartz Tom Phoenix, "Learning PERL", Oreilly Publications, 3rd Edn., 2000
2. Larry Wall, Tom Christiansen, John Orwant, "Programming PERL", Oreilly Publications, 3rd Edn., 2000.
3. Tom Christiansen, Nathan Torkington, "PERL Cookbook", Oreilly P

VLSI DESIGN LAB - I

1. Digital Circuits Description using Verilog
2. Verification of the Functionality of Designed circuits using function Simulator.
3. Timing simulation for critical path time calculation.
4. Synthesis of Digital circuits.
5. Place and Route techniques for major FPGA vendors such as Xilinx, Altera and Actel etc.
6. Implementation of Designed Digital Circuits using FPGA and CPLD devices.

NOTE: Required Software Tools:
1**.** Mentor Graphic tools / Cadance tools/ Synophysis tools. (220 nm Technology and Above)
2. Xilinx 11.1i and Above for FPGA/CPLDS / FPGA Advantage.

TESTING & TESTABILITY

UNIT I

INTRODUCTION TO TEST AND DESIGN FOR TESTABILITY (DFT) FUNDAMENTALS: Modeling: Modeling Digital Circuits at Logic Level, Register Level and Structural Models. Levels of Modeling. Logic Simulation: Types of Simulation, Delay Models, Element Evaluation, Hazard Detection, Gate Level Event Driven Simulation.

UNIT II

FAULT MODELING: Logic Fault Models, Fault Detection and Redundancy, Fault Equivalence and Fault Location. Single Stuck and Multiple Stuck – Fault Models. Fault Simulation Applications, General Techniques for Combinational Circuits.

UNIT III

TESTING FOR SINGLE STUCK FAULTS (SSF): Automated Test Pattern Generation (ATPG/ATG) For Ssfs In Combinational and Sequential Circuits, Functional Testing With Specific Fault Models, Test Pattern Generation, Compression Techniques – Different Techniques, Syndrome Test and Signature Analysis.

UNIT IV

DESIGN FOR TESTABILITY: Testability Trade-Offs, Techniques. Scan Architectures and Testing – Controllability and Absorbability, Generic Boundary Scan, Full Integrated Scan, Storage Cells for Scan Design. Board Level and System Level DFT Approaches. Boundary Scans Standards

UNIT V

BUILT-IN SELF-TEST (BIST): BIST Concepts, Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief Ideas on Some Advanced BIST Concepts and Design for Self-Test at Board Level, ICT, JTAG Testing Features.

TEXT BOOKS:

1. Miron Abramovici, Melvin A. Breur, Arthur D.Friedman, Digital Systems Testing and Testable Design, Jaico Publishing House, 2001.

REFERENCES:

1. Alfred Crouch, Design for Test for Digital ICs & Embedded Core Systems, Prentice Hall.
2. Robert J.Feugate, Jr., Steven M.Mentyn, Introduction to VLSI Testing, Prentice Hall, Englehood Cliffs, 1998.

LOW POWER VLSI DESIGN

UNIT I

LOW POWER DESIGN, AN OVER VIEW: Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.

MOS/BiCMOS PROCESSES: Bi-CMOS processes, Integration and Isolation considerations, Integrated Analog/Digital CMOS Process.

UNIT II

LOW-VOLTAGE/LOW-POWER CMOS/BICMOS PROCESSES: Deep submicron processes, Low Voltage/Low power CMOS/BiCMOS processes, future trends and directions of CMOS/Bi-CMOS processes.

UNIT III

DEVICE BEHAVIOR AND MODELING: MOSFET SPICE models, Advanced MOSFET Models, limitations of MOSFET models, Bi-polar models.

UNIT IV

LOW- VOLTAGE LOW POWER LOGIC CIRCUITS: Conventional CMOS and Bi-CMOS logic gates,

Advanced Bi-CMOS Digital circuits – BiCMOS Circuits Utilizing Lateral pnp BJTs in PMOS Structures, Merged BiCMOS Logic Circuits, Full-Swing Multidrain/Multicollector Complementary BiCMOS Buffers, Quasi-Complementary BiCMOS Digital Circuits, ESD-free Bi-CMOS Digital circuit.

UNIT V

LOW POWER LATCHES AND FLIP FLOPS: Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

SPECIAL TECHNIQUES: Power Reduction in Clock Networks, CMOS Floating Node, Low Power Bus, Delay Balancing, Low Power Techniques for SRAM.

TEXT BOOKS:

1. Yeo Rofail/ Gohl(3 Authors), "CMOS/BiCMOS ULSI low voltage, low power", Pearson Education Asia 1st Indian reprint,2002.
2. Gary K. Yeap,"Practical Low Power Digital VLSI Design", KAP, 2002.

REFERENCES:

1. Douglas A.Pucknell & Kamran Eshraghian, "Basic VLSI Design", 3rd edition PHI.
2. J.Rabaey, "Digital Integrated circuits", PH,1996
3. Sung-mo Kang and yusuf leblebici, "CMOS Digital ICs", 3rd edition TMH 2003 .
4. IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia.

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES::RAJAMPET
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M.Tech (VLSI SYSTEM DESIGN) II SEMESTER

HARDWARE SOFTWARE CO-DESIGN

UNIT I:

ESSENTIAL ISSUES IN CODESIGN: Models, Architectures, Languages and Generic codesign methodology

CO-SYNTHESIS ALGORITHMS: Architectural Models, Hardware/Software Partitioning, Distributed system co-synthesis

UNIT II

PROTOTYPING AND EMULATION: Techniques, Environments and future developments

TARGET ARCHITECTURE: Architecture specialization Techniques, system communication infrastructure, Target Architectures and application system classes, Architectures for control-dominated systems, Architectures for data dominated systems, Mixed systems and Less specialized systems

UNIT III

COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES: Modern Embedded Architectures, Embedded software development needs, Compiler Technologies, practical considerations in a compiler development environment

UNIT IV

DESIGN SPECIFICATION AND VERIFICATION: Design, Co-design, co-design computational model, Concurrency, Coordinating concurrent computations, Interfacing Components, Verification.

UNIT V

LANGUAGES FOR SYSTEM LEVEL SPECIFICATION AND DESIGN: System level specification, Design representation for system level synthesis, System level specification languages, Heterogeneous specification and multi-language co-simulation

TEXT BOOK:

1. Jorgen Staunstrup, Wayne Wolf, "Hardware/Software Co-Design: Principles and Practice" Springer, fourth Indian reprint, 2013.

ANNAMACHARYA INSTITUTE OF TECHNOLOGY AND SCIENCES, RAJAMPET
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M.Tech (VLSI SYSTEM DESIGN) II Semester

ASIC DESIGN

UNIT I

ASIC DESIGN STYLES: Introduction – categories-Gate arrays-Standard cells-Cell based ASICs-Mixed mode and analogue ASICs – PLDs.

UNIT II

ASICS – PROGRAMMABLE LOGIC DEVICES: Overview – PAL –based PLDs: Structures; PAL Characteristics – FPGAs: Introduction, selected families – design outline.

ASICS –DESIGN ISSUES: Design methodologies and design tools – design for testability – economies.

UNIT III

ASICS- CHARACTERISTICS AND PERFORMANCE: design styles, gate arrays, standard cell -based ASICs, Mixed mode and analogue ASICs.

UNIT IV

ASICS-DESIGN TECHNIQUES: Overview- Design flow and methodology-Hardware description languages-simulation and checking-commercial design tools- FPGA Design tools: XILINX, ALTERA

LOGIC SYNTHESIS, SIMULATION AND TESTING: Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation-automatic test pattern generation.

UNIT V

ASIC CONSTRUCTION: Floor planning, placement and routing system partition.

FPGA PARTITIONING: Partitioning Methods-Floor Planning- Placement-Physical Design Flow-Global Routing-Detailed Routing –Special Routing-Circuit Extraction-DRC.

TEXT BOOKS:

1. L.J.Herbst,"Integrated circuit engineering", OXFORD SCIENCE Publications, 1996.

REFERENCES:

1. M.J.S.Smith, "Application - Specific integrated circuits", Addison-Wesley Longman Inc 1997.

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M.Tech (VLSI SYSTEM DESIGN) II Semester

ALGORITHMS FOR VLSI DESIGN AUTOMATION

UNIT I

PRELIMINARIES AND GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION: Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems, Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT II

MODELLING AND SIMULATION: Gate Level Modeling and Simulation, Switch level Modeling and Simulation.

UNIT III

LOGIC SYNTHESIS AND VERIFICATION: Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis- Problem Definition and Analysis.

UNIT IV

HIGH-LEVEL SYNTHESIS: Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, ASAP and mobility based scheduling algorithms , Some aspects of Assignment problem, High-level Transformations.

UNIT V

PHYSICAL DESIGN AUTOMATION OF FPGA'S AND MCM'S : FPGA technologies, Physical Design cycle for FPGA's, partitioning and Routing for segmented and staggered Models, MCM technologies, MCM physical design cycle, Partitioning, Placement- Chip Array based and Full Custom Approaches, Routing, Maze routing, Multiple stage routing, Topologic routing, Integrated Pin, Distribution and routing, Routing and Programmable MCM's.

TEXTBOOKS:

1. S.H.Gerez, "Algorithms for VLSI Design Automation", WILEY Student Edition, John wiley & Sons (Asia) Pvt. Ltd., 1999.
2. Naveed Sherwani, "Algorithms for VLSI Physical Design Automation" ,3rd edition, Springer International Edition, 2005.

REFERENCES:

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, Wiley, 1993.
2. Modern VLSI Design Systems on silicon – Wayne Wolf, Pearson Education Asia, 2nd Edition, 1998.

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M.Tech (VLSI SYSTEM DESIGN) II Semester

NANO ELECTRONICS
ELECTIVE II

UNIT I
TECHNOLOGY AND ANALYSIS:
Film Deposition Methods, Lithography, Material Removing Technologies, Etching and Chemical, Mechanical Processing, Scanning Probe Techniques.

CARBON NANO STRUCTURES: Carbon Clusters, Carbon Nano tubes, Fabrication, Electrical, Mechanical and Vibrational Properties, Applications of Carbon Nano Tubes.

UNIT II
LOGIC DEVICES: Silicon MOSFETS, Novel Materials and Alternative Concepts, Ferro Electric Filed Effect Transistors, Super Conductor Digital Electronics, Carbon Nano Tubes for Data Processing.

UNIT III
RADOM ACESS MEMORIES: High Permitivity Materials for DRAMs, Ferro Electric Random Access Memories, Magneto-Resistive RAM.

UNIT IV
MASS STORAGE DEVICES:
Hard Disk Drives, Magneto Optical Disks, Rewriteable DVDs based on Phase Change Materials, Holographic Data Storage.

UNIT V
DATA TRANSIMISSION, INTERFACES AND DISPLAYS:
Photonic Networks, Microwave Communication Systems, Liquid Crystal Displays, Organic Light Emitting Diodes.

TEXTBOOKS:
1. Rainer Waser, "Nano Electronics and Information Technology", Wiley VCH, April 2003.
2. Charles Poole, "Introduction to Nano Technology", Wiley Interscience, May 2003

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M.Tech (VLSI SYSTEM DESIGN) II Semester

VLSI Signal Processing
ELECTIVE II

UNIT I

INTRODUCTION TO DSP SYSTEMS

Introduction To DSP Systems -Typical DSP algorithms; Iteration Bound – data flow graph representations, loop bound and iteration bound, Longest path Matrix algorithm; Pipelining and parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.

UNIT II

RETIMING

Retiming - definitions and properties; Unfolding – an algorithm for Unfolding, properties of unfolding, sample period reduction and parallel processing application; Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT algorithm architecture transformation, parallel architectures for rank-order filters, Odd- Even Merge- Sort architecture, parallel rank-order filters.

UNIT III

FAST CONVOLUTION

Fast convolution – Cook-Toom algorithm, modified Cook-Took algorithm; Pipelined and parallel recursive and adaptive filters – inefficient/efficient single channel interleaving, Look- Ahead pipelining in first- order IIR filters, Look-Ahead pipelining with power-of-two decomposition, Clustered Look-Ahead pipelining, parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters, pipelined adaptive digital filters, relaxed look-ahead, pipelined LMS adaptive filter.

UNIT IV

BIT-LEVEL ARITHMETIC ARCHITECTURES

Scaling and roundoff noise- scaling operation, roundoff noise, state variable description of digital filters, scaling and roundoff noise computation, roundoff noise in pipelined first-order filters; Bit-Level Arithmetic Architectures- parallel multipliers with sign extension, parallel carry-ripple array multipliers, parallel carry-save multiplier, 4x 4 bit Baugh- Wooley carry-save multiplication tabular form and implementation, design of Lyon’s bit-serial multipliers using Horner’s rule, bit-

serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement.

UNIT V
PROGRAMMING DIGITAL SIGNAL PROCESSORS

Numerical Strength Reduction – sub expression elimination, multiple constant multiplications, iterative matching. Linear transformations; Synchronous, Wave and asynchronous pipelining-synchronous pipelining and clocking styles, clock skew in edge-triggered single-phase clocking, two-phase clocking, wave pipelining, asynchronous pipelining bundled data versus dual rail protocol; Programming Digital Signal Processors – general architecture with important features; Low power Design – needs for low power VLSI chips, charging and discharging capacitance, short-circuit current of an inverter, CMOS leakage current, basic principles of low power design.

REFERENCES

1. Keshab K.Parhi, "VLSI Digital Signal Processing systems, Design and implementation", Wiley, Inter Science, 1999.
2. Gary Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Publishers, 1998.
3. Mohammed Isamail and Terri Fiez, "Analog VLSI Signal and Information Processing", Mc Graw-Hill, 1994.
4. S.Y. Kung, H.J. White House, T. Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1985.
5. Jose E. France, Yannis Tsividis, "Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994.

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M.Tech (VLSI SYSTEM DESIGN) II Semester
DSP PROCESSORS & ARCHITECTURES
ELECTIVE - II

UNIT I

INTRODUCTION TO DIGITAL SIGNAL PROCESING: Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS: Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT II

ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT III

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS: Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

UNIT IV

IMPLEMENTATIONS OF BASIC DSP ALGORITHMS: The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

IMPLEMENTATION OF FFT ALGORITHMS: An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

UNIT V

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES: Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS:

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. DSP Processor Fundamentals, Architectures & Features – Lapsley et al.S. Chand & Co, 2000.

REFERENCES:

1. Digital Signal Processors, Architecture, Programming and Applications-B.Venkata Ramani and M. Bhaskar, TMH, 2004.
2. Digital Signal Processing – Jonatham Stein, John Wiley, 2005.

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M.Tech (VLSI SYSTEM DESIGN) II Semester

VLSI DESIGN LAB - II

1. Analog Circuits Simulation using Spice.
2. Mixed Signal Simulation Using Mixed Signal Simulators.
3. Layout Extraction for Analog & Mixed Signal Circuits.
4. Parasitic Values Estimation from Layout.
5. Layout Vs Schematic.
6. Net List Extraction.
7. Design Rule Checks.

NOTE: Required Software Tools:
1**.** Mentor Graphic tools / Cadance tools/ Synophysis tools. (220 nm Technology and Above)
2. Xilinx 9.1i and Above for FPGA/CPLDS.