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(19) INDIA
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(43) Publication Date : 25/12/2020

(54) Title of the invention : SYSTEM AND A METHOD FOR AN INTELLIGENT/AUTOMATIC TUNING OF POWER CONVERTER OF ELECTRIC VEHICLE FOR CHARGING THE BATTERY THEREOF

| | |
|---|---|
| (51) International classification | :B60L 53/30 |
| (31) Priority Document No | :NA |
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| (61) Patent of Addition to Application Number<br>Filing Date | :NA<br>:NA |
| (62) Divisional to Application Number<br>Filing Date | :NA<br>:NA |

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**3)Dr.P.BALACHENNAIAH**
**4)Dr. K. AMARESH**
**5)S. MUQTHIAR ALI**
**6)Dr.S.JEYASUDHA**
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**4)Dr. K. AMARESH**
**5)S. MUQTHIAR ALI**
**6)Dr.S.JEYASUDHA**

(57) Abstract :
ABSTRACT OF THE INVENTION Nowadays the electric vehicles are so popular and occupying the roads in pace manner. Different manufacturers are involving in the electric vehicles manufacturing business and making different kind of electric vehicles with unique technology and elements. Charging stations are plays a vital role in refilling the energy to the storage unit of the vehicle. Each manufacturer adopting the battery in their vehicle with different rating due to which it is difficult to charge the battery with an appropriate voltage and current values. This issue has been addressed through this invention. The ways and means of charging the battery in electric vehicle is proposed here so as to improve the battery performance and its reliability. While purchase the electric vehicle, the electric vehicle and battery details such as battery make, manufacturing year, type & ratings such as voltage, Ampere hour (Ah) are send to the IoT database. The IoT is universally permitted to assess by all the charging stations. While charging the electric vehicle at the charging station, the information on the battery is sensed through its communication channel and verified with the database available in IoT. And at the same time, the information on the battery and vehicle is also transferred and or stored in the local controller which located at the charging station. The communication between the charging station and the local control unit is made through wireless or wired mode based on the convenience. Local control unit has the memory and the programme which decides the value of duty cycle of the charging converter. The DC charging unit has the capability of both slow and fast charging and it is supplied with either or both renewable energy source and the grid. The local control unit sends the signal to the DC charging unit and accordingly the appropriate ad hoc firing pulses are generated so that the charging parameters like voltage and current which matching with the battery are fixed and the estimated charging time is informed to the customer. These parameters are fixed based on the type, condition and past history of battery charging time for full charge. This invention breaks the existing charging methodology and enhances the performance of electric vehicle™s battery.

No. of Pages : 12 No. of Claims : 7

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सत्यमेव जयते

INTELLECTUAL PROPERTY INDIA
PATENTS | DESIGNS | TRADE MARKS
GEOGRAPHICAL INDICATIONS

**G.A.R.6**
**[See Rule 22(1)]**
**RECEIPT**

**Docket No 14693** **Date/Time 2021/02/19 09:57:21**

**To**
**NAGARAJAN NANDHAN**

**UserId: NaguKalpu**

**2/72 BAZAAR STREET ADHIYAMAN**
**KOTTAI POST VAO OFFICE NEAR**

**CBR Detail:**

| Sr. No. | Ref. No./Application No. | App. Number | Amount Paid | C.B.R. No. | Form Name | Remarks |
|---|---|---|---|---|---|---|
| 1 | E-12/636/2021/CHE | 202141006933 | 2500 | 6018 | FORM 9 | |
| 2 | 202141006933 | TEMP/E-1/6771/2021-CHE | 1760 | 6018 | FORM 1 | A LOW COST PORTABLE EARTH DETECTING SAFETY PLUG POINT |

| TransactionID | Payment Mode | Challan Identification Number | Amount Paid | Head of A/C No |
|---|---|---|---|---|
| N-0000763347 | Online Bank Transfer | 1902210001233 | 4260.00 | 1475001020000001 |

Total Amount : ₹ 4260
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## Design Application Details

**Application Number:**

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**Cbr Number:**

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**Cbr Date:**

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**Applicant Name:**

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**3. Dr. LUKE JOHN BAKTHA SINGH IMMARAJU** **4. Dr. BOLLA MADHUSUDHANA REDDY**
**5. PALLETI VENKATA KUSUMA** **6. M. MANIKUMAR REDDY**
**7. KAMESWARA VASISHTA KUMAR KAVUTURU** **8. Dr. V. LAKSHMI DEVI**
**9. Dr. VARAPRASAD JANAMALA** **10. Dr. KORITALA CHANDRA SEKHAR**

## Design Application Status

**Application Status:**

Application Under Process(Awating for Technical Examination)

Back (/designapplicationstatus/)

(71) Syngen Biotech Co., Ltd.
(21) 2021102354 (22) 04.05.2021
(54) Fermented dragon fruit powder for improving enteritis and preventing colorectal cancer and preparation method thereof

**T, R. see Rajathi, G.I.**
(21) 2021102408

**T., A. see Rajathi, G.I.**
(21) 2021102408

(54) Classification system and automatic scoring method of condition of adult emergency case

**Thorat, M. see Raut, R.**
(21) 2021102390

**THOTA, S. see REDDY, R.**
(21) 2021102414

(71) Tianjin Eye Hospital
(21) 2021102331 (22) 03.05.2021
(54) PERIPHERAL RETINAL ABERRATION OPTICAL MEASUREMENT DEVICE

**T R, R. see Benal, M.M.**
(21) 2021102375

**Tripathi, A.O. see Chawda, D.R.**
(21) 2021102344

**Tripathi, A. see Ghorpade, N.**
(21) 2021102450

**Tripathy, R. see Hussain, M.I.**
(21) 2021102374





## Innovation Patent Applications Filed - Name Index cont'd

(71) V, T.K.G.; Gannavaram, V.C.S.; Gannavaram, V.P.; Ganta, R.R.; Sakimalla Prabhakar, G.; Kama, R.; Budda, J.K.; Vadithala, C.S.R.; Vuppu, S.; Chintakindi, S.; Manchala Sashi Bushan, P.; Pratapagiri, S.; Kollun, J.
(21) 2021102330 (22) 03.05.2021
(54) SOLAR PARK MONITORING AND FAULT DETECTION SYSTEM USING IOT AND MACHINE LEARNING

**Vadithala, C.S.R. see V, T.K.G.**
(21) 2021102330

(71) VASU, G.; Kumar, M.S.; Raju, M.R.
(21) 2021102341 (22) 03.05.2021
(54) A model order reduction method for optimal model approximation of linear-time invariant systems

(71) Vbreathe Pty Ltd
(21) 2021102443 (22) 10.05.2021
(54) Apparatus for Air Cleaning
(62) 2017383090

**Venkatesan, M. see Kumar Jain, J.**
(21) 2021102408

**Verma, S. see Narasimhulu, C.V.**
(21) 2021102424

**Verma, S. see Vyas, A.**
(21) 2021102426

(71) VERMA, B.K.; Dongre, S.; Sashibhushan, S.; Rai, B.K.; Kamboj, P.; Sharma, A.; Sharma, D.M.; Prasad, D.; Pattnaik, B.
(21) 2021102340 (22) 03.05.2021
(54) ANALYSIS OF HEATH CARE CHATBOT USING ARTIFICIAL INTELLIGENCE TECHNIQUES

(71) Versan Management Pty Ltd
(21) 2021102367 (22) 05.05.2021
(54) A Multipurpose Towel
(31) 2020901774 (32) 29.05.20 (33) AU

**V G, B. see Benal, M.M.**
(21) 2021102375

**VIDYA RAJ, C. see SENGOTTUVELAN, P.**
(21) 2021102413

**Vijayanand, S. see Balakrishna, R.**
(21) 2021102421

**Vuppu ... V, T.K.G.**
(21) ...102330

(71) Vyas, A.; Lalitha, M.P.; Babu, U.R.; Bhalerao, R.S.; ..., K.; Verma, S.; Dash, S.; Choudhury, N.B.D.; Tiwari, M.; Thakkar, R.R.
(21) 2021102426 (22) 09.05.2021
(54) Internet of Things Based Automatic Railway Gate Controller

(71) Waghulde, K.B.; Patil, A.A.; Desh... Choudhary, A.S.; Pat... ...ail, T.N.; ... ...kar, B.K.
(21) 2021102423 (22) 09.05.2021
(54) Pesticide Sprayer & COVID Sanitization Intelligent Drone

(71) WEIFANG MEDICAL UNIVERSITY
(21) 2021102399 (22) 07.05.2021
(54) BERBERINE/MINERALIZED COLLAGEN-BASED COMPOSITE MEMBRANE AND PREPARATION METHOD AND APPLICATION THEREOF
(31) 202011317356.X (32) 23.11.20 (33) CN

(71) Wenzhou-Kean University
(21) 2021102398 (22) 07.05.2021
(54) A Combination Drug of Human Interferon-ε and Interferon-γ

(71) West China Hospital, Sichuan University
(21) 2021102332 (22) 03.05.2021
(54) DEVICE FOR TESTING COGNITIVE ABILITY OF TUPAIA BELANGERI

(71) Wuhan University
(21) 2021102442 (22) 10.05.2021
(54) METHOD FOR REINFORCING COLUMN WITH A SLEEVED EXTERNALLY THIN-WALLED STEEL TUBE AND SELF-COMPACTING CONCRETE

**XIAMEN UNIVERSITY see Beijing NATON Technology Group Co., Ltd**
(21) 2021102400

(71) Xiangtan University
(21) 2021102459 (22) 11.05.2021
(54) OBSERVABLE MICRO-NANO MECHANICAL TESTING APPARATUS AND METHOD
(31) 202011586567.3 (32) 29.12.20 (33) CN

(71) Yan'an Hospital of Kunming City
(21) 2021102402 (22) 07.05.2021
(54) IMPROVED DENTAL CURET FOR DEPARTMENT OF STOMATOLOGY
(31) 202010566240.5 (32) 17.06.20 (33) CN

(71) Yellow Sea Fisheries Research Institute, Chinese Academy of Fishery Sciences
(21) 2021102452 (22) 11.05.2021
(54) Detection Method of Inorganic Lead Ions in Marine Shellfish by HPLC-ICP-MS Technique

**...an, X. see Li, Z.**
(21) 2021102434

(71) Zhejiang Institute of Garden Plants and Flowers (Zhejiang Xiaoshan Institute of Cotton & Bast Fiber Crops Research)
(21) 2021102470 (22) 11.05.2021
(54) DROUGHT AND HIGH-SALT RESISTANT PROMOTER OF PAEONIA SUFFRUTICOSA PSDREB1 GENE AND EXPRESSION AND USE THEREOF

**Zhengzhou Zhongdao Biotechnology. Co. LTD see Institute of Animal Health, Guangdong Academy of Agricultural Sciences**
(21) 2021102363

(71) Zhongda Testing (Hunan) Co., Ltd.
(21) 2021102359 (22) 05.05.2021
(54) WIRELESS INCLINOMETER
(31) 202011103671.2 (32) 15.10.20 (33) CN





## Numerical Index

Office of the Controller General of Patents, Designs & Trade Marks
Department of Industrial Policy & Promotion,
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| Application Details | |
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| APPLICATION NUMBER | 202141016273 |
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| DATE OF FILING | 07/04/2021 |
| APPLICANT NAME | 1 . Dr. D. R. SRINIVASAN<br>2 . Dr. P. VEERA SANJEEVA KUMAR<br>3 . Dr. RAM SUBBIAH<br>4 . Mr. S. VETRIVEL<br>5 . Dr. A. RAMESH KUMAR<br>6 . Mr.N. NAGARAJAN |
| TITLE OF INVENTION | SEMI AUTOMATIC PNEUMATIC POWERED ROD BENDING MACHINE USING SOLENOID VALVE |
| FIELD OF INVENTION | MECHANICAL ENGINEERING |
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| Application Status | |
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| APPLICATION STATUS | Awaiting Request for Examination |

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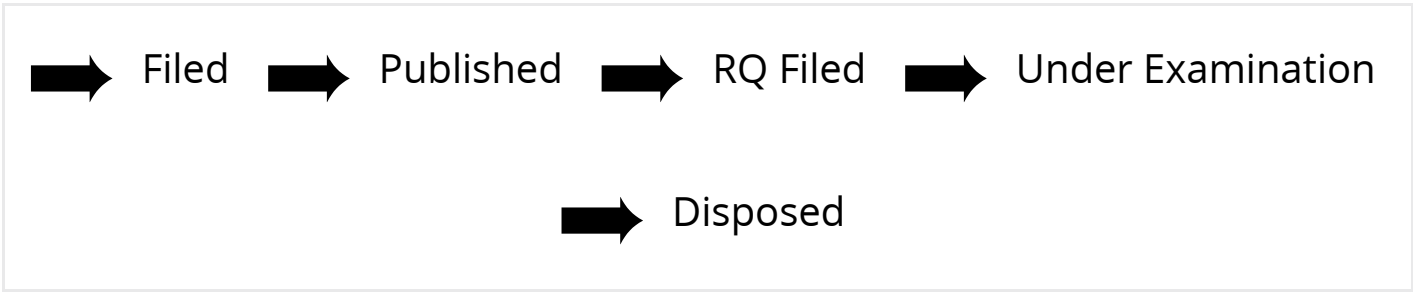
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(54) Title of the invention : PERFORMANCE OPTIMIZATION OF RECONFIGURABLE MANUFACTURING SYSTEM USING DUAL STEP METAHEURISTIC APPROACH

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| (51) International classification | :G06Q0010040000, G06Q0050060000, G06Q0010060000, G06F0111060000, G06F0030170000 |
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**2)Dr N Chikkanna**
**3)Puneet Shetteppanavar**

(57) Abstract :
TITLE OF INVENTION: Performance Optimization of Reconfigurable Manufacturing System Using Dual Step Metaheuristic Approach Field of Invention: Mechanical Engineering ABSTRACT Reconfigurable manufacturing system aka RMS is a novice topology in manufacturing sector that is designed in accordance with the product requirement, however re-configurability is considered as the non-functional system requirement and it is long term behavior. Thus considering the conventional approach dynamic change is highly improbable; hence it is necessary to design the model that has the dynamic change capacity. In this Invention, we have developed (DSMO) dual step metaheuristic optimized approach to solve the two distinctive problem; in first step we optimize the product changes reaction. In second step, we develop the optimized layout for machine selection by optimizing the machine floor arrangement and position of machine. Further dual step mechanism is evaluated through comparison analysis with the existing model of ANC90. Moreover, evaluation is performed by considering two cases adopted from the existing model; in case 1 cost comparison has been carried out whereas in case 2 re-configuration cost, total cost and capital cost are compared. Further comparison has been carried out considering the various scenarios in both cases and comparative analysis indicates that proposed methodologies simply outperforms the existing model.

No. of Pages : 11 No. of Claims : 1

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Department of Industrial Policy & Promotion,
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| DATE OF FILING | 07/04/2021 |
| APPLICANT NAME | 1 . Dr. D. R. SRINIVASAN<br>2 . Dr. P. VEERA SANJEEVA KUMAR<br>3 . Dr. RAM SUBBIAH<br>4 . Mr. S. VETRIVEL<br>5 . Dr. A. RAMESH KUMAR<br>6 . Mr.N. NAGARAJAN |
| TITLE OF INVENTION | SEMI AUTOMATIC PNEUMATIC POWERED ROD BENDING MACHINE USING SOLENOID VALVE |
| FIELD OF INVENTION | MECHANICAL ENGINEERING |
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| APPLICATION STATUS | Awaiting Request for Examination |

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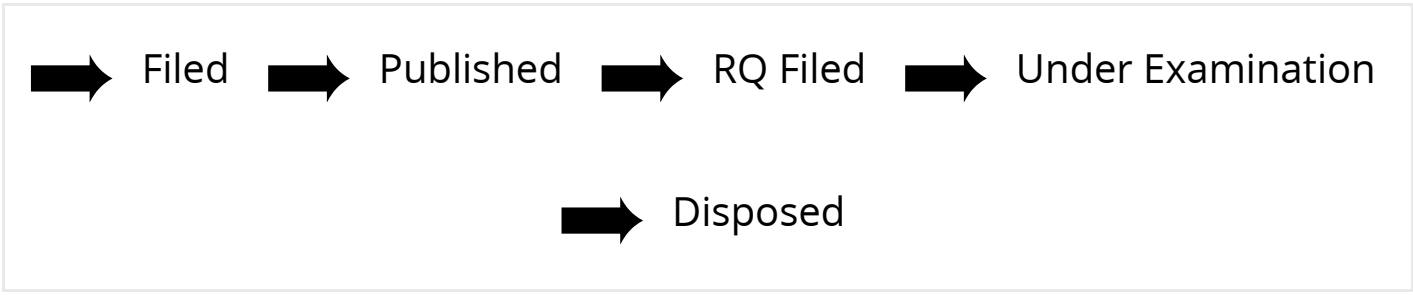
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(19) INDIA
(22) Date of filing of Application :02/05/2021

(21) Application No.202141020084 A
(43) Publication Date : 07/05/2021

(54) Title of the invention : A NOVEL METHOD AND SYSTEM FOR DESIGNING VLSI CIRCUITRY TO OPTIMIZE THE INTEGRATED CIRCUIT OPERATION

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| (51) International classification | :G06F0030394000, G06F0030392000, H01S0005100000, H01S0005020000, H01L0023000000 |
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**7)Mr.G.Ravi**
**8)Dr D.Thirumal Reddy**
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**10)Mr.Shaik Karimullah**

(57) Abstract :
ABSTRACT A NOVEL METHOD & SYSTEM FOR DESIGNING VLSI CIRCUITRY TO OPTIMIZE THE INTEGRATED CIRCUIT OPERATION [031] The present invention discloses a system for designing VLSI circuitry. The system includes, but not limited to a top semiconductor layer constructed with a material with a higher resistivity and a higher transparency properties; a routing area having a plurality of component tiles positioned thereon; a means configured for reconfiguring the component tiles, enabling the design into a maximal component tiles and a maximal space tiles; and a processor for providing the instructions while designing and constructing the top semiconductor layer, the routing area, the component tiles and maximal space tiles. Accompanied Drawing [FIGS. 1 & 2]

No. of Pages : 21 No. of Claims : 7

Australian Government

IP Australia

# CERTIFICATE OF GRANT

# INNOVATION PATENT

**Patent number:** 2021100880

The Commissioner of Patents has granted the above patent on 7 April 2021, and certifies that the below particulars have been registered in the Register of Patents.

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**Title of invention:**

AN ARTIFICIAL NEURAL NETWORK SYSTEM FOR FUNCTIONAL MRI SEGMENTATION WITH CC-BPA

**Name of inventor(s):**

H.N., Reddappa; Lingam, K. Mallikarjuna; Shet K., Sathisha; B. B., Shankar; Kuncha, Prathyusha; Misra, Alok; Tumula, Durga Prasad; Kumar D.R.V.A, Sharath; Kumar, S. Praveen; Gopinadh, R.; Brundavani, P. and Vardhan, D. Vishnu

**Term of Patent:**

Dated this 7th day of April 2021

Commissioner of Patents

COMMONWEALTH OF AUSTRALIA AUSTRALIA PATENT OFFICE

PATENTS ACT 1990

The Australian Patents Register is the official record and should be referred to for the full details pertaining to this IP Right.

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(22) Date of filing of Application :02/02/2021

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(54) Title of the invention : A NOVEL METHOD OF DESIGN OF LOW POWER VLSI BASED VITERBI DECODER USING GATE DIFFUSION INPUT

| | |
|---|---|
| (51) International classification | :H03M0013410000, H04L0001000000, H03M0013000000, H03M0013230000, H03M0013350000 |
| (31) Priority Document No | :NA |
| (32) Priority Date | :NA |
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**5)Dr.G.MadhusudhanaRao**
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**6)Mr.A.Manoharan**
**7)Mr.Anup D Bhange**
**8)Mr.Shaik Karimullah**
**9)Mr.Syed Javeed Basha**
**10)Mr.K.Tarakeswara Rao**

(57) Abstract :
The Error Control mechanism in Digital Wireless Communication can be performed with error detection and correction. The Viterbi Decoder is used for detecting and correcting the Errors in Digital Wireless Communication. The Channel Coding is the most important coding performed at the receiver of the Digital Wireless Communication channel. The Convolutional Codes are most commonly used in the channel codding of the Digital Wireless Communication channel which are decoded by the Viterbi Decoder. The present invention disclosed herein is a Novel Method of Design of Low Power VLSI based Viterbi Decoder using Gate Diffusion Input comprising of: Branch Metric Unit (301); 3-Bit Adder (302); 4-Bit Comparator (303); 4-Bit Selector (304); and Survivor Memory Unit (305); facilitates an efficient low power design architecture for the Viterbi Decoder. In the present invention disclosed herein, the power consumption is reduced due to its optimum design over 29% at 24MHz clock frequency compared to the standard CMOS design. The area of the decoder with Gate Diffusion Input reduced over 70% than the CMOS design, and the transition delay reduced by 1.5 times than the decoder designed with CMOS logic. The present invention disclosed herein is designed on the Tanner Simulation Program with Integrated Circuit Emphasis in 0.251'm technology, Vdd =2.5V and Clock frequency is 24MHz.

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(21) Application No.202141006425 A
(43) Publication Date : 19/02/2021

(54) Title of the invention : A NOVEL METHOD OF POWER REDUCTION IN MODIFIED AES USING BIT ENCRYPTION AND DECRYPTION TRANSITION SCHEME ON FPGA

| | |
|---|---|
| (51) International classification | :H04L0009060000, H04L0029060000, H04L0009000000, H04B0010850000, H04L0001160000 |
| (31) Priority Document No | :NA |
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| (33) Name of priority country | :NA |
| (86) International Application No<br>Filing Date | :NA<br>:NA |
| (87) International Publication No | : NA |
| (61) Patent of Addition to Application Number<br>Filing Date | :NA<br>:NA |
| (62) Divisional to Application Number<br>Filing Date | :NA<br>:NA |

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(57) Abstract :
The data such as text, Image, and Video can be transmitted by the communication systems from one node to another node. While transmitting the data, the security is utmost concern and is obtained by the Data Encryption and Data Decryption. The increased Speed of Data transmission and the less utilization of power are the factors to be considered while designing the communication system with VLSI Technology. The implementation of Advanced Encryption Standard (AES) on the Field Programmable Gate Array (FPGA) is highly flexible and efficient method for high secured data encryption and decryption system. The implementation of Modified AES on FPGA is having more number of transitions due to continuously receiving data and continuously transmitting the data. The power consumption is more in implementation of Modified AES on FPGA, can be optimized and reduced with the Bit Encryption and Decryption Transition Scheme. The present invention disclosed here is a Novel Method of Power Reduction in Modified AES using Bit Encryption and Decryption Transition Scheme on FPGA comprising of: Data Input (201); Key Input (202); BEDT Scheme (203); S-Box Generation (204); Row Shift (205); Steller Matrix (206); Inverse BEDT (207); Inverse S-Box (208); Row Shift (209); Steller Matrix (210); Decrypted Data (211); reduces the power in modified Advanced Encryption Standard implemented on FPGA. The present invention disclosed here reduces the power to 0.42mw for 325 flip flop pairs in the design. The present invention is implemented on the Verilog HDL programming on the Virtex-5 FPGA Development Board.

No. of Pages : 15 No. of Claims : 5

(12) PATENT APPLICATION PUBLICATION
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(22) Date of filing of Application :28/11/2020

(21) Application No.202041051968 A
(43) Publication Date : 11/12/2020

(54) Title of the invention : ENHANCEMENT OF QUALITY OF SERVICE IN WIRELESS SENSOR NETWORK BY REDUNDANT SENSORS CONTROLLING

| | |
|---|---|
| (51) International classification | :H04W 84/18 |
| (31) Priority Document No | :NA |
| (32) Priority Date | :NA |
| (33) Name of priority country | :NA |
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| Filing Date | :NA |

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(57) Abstract :
Wireless Sensor Network contains randomly distributed Sensors which are tiny through which the data is transmitted or services are provided to the end users. The Quality of Service (QoS) depends on these sensors deployment to overcome the redundancy in the network. The present invention disclosed here is Enhancement of Quality of Service in Wireless Sensor Network by Redundant Sensors Controlling comprising of: Deployment of Sensors (201); Network Parameters (202); Fuzzy Controller (203); Protocol (204); improves the quality of service by controlling the redundant sensors in the wireless network. The redundant sensors are analysed and controlled by the Fuzzy logic. The energy consumed by the Redundant Sensor Nodes is reduced by the Adaptive Clustering Hierarchy Redundancy Aware Protocol (ACH-RAP) to increase the network lifetime.

No. of Pages : 14 No. of Claims : 6

(12) PATENT APPLICATION PUBLICATION
(19) INDIA
(22) Date of filing of Application :28/12/2019
(21) Application No.201941054297 A
(43) Publication Date : 09/10/2020

(54) Title of the invention : SELF-RELIABILITY BASED WEIGHTED SOFT-BIT-FLIPPING ALGORITHM FOR DECODING EG-LDPC CODES

| | |
|---|---|
| (51) International classification | :H03M0013110000, H03M0013000000, H03M0013370000, H03M0013390000, H04L0001000000 |
| (31) Priority Document No | :NA |
| (32) Priority Date | :NA |
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| (86) International Application No<br>Filing Date | :NA<br>:NA |
| (87) International Publication No | : NA |
| (61) Patent of Addition to Application Number<br>Filing Date | :NA<br>:NA |
| (62) Divisional to Application Number<br>Filing Date | :NA<br>:NA |

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(57) Abstract :
The conventional algorithms such as Soft-Bit Flipping (SBF) algorithm, Majority Logic Decoder/Detector (MLDD) algorithm, Sequential Peeling Decoder (SPD) algorithm, Parallel Peeling Decoder (PPD) algorithm, Belief Propagation Decoder (BPD) attain the satisfactory decoding performance in terms of error correction and detection. For the standard conventional algorithms, a lot of multiplicative and logarithmic computations are required for the check node computation. Hence, the decoding latency, hardware complexity and power consumptions of the standard conventional algorithms are high due to their complex computation process. The proposed Self-Reliability based Weighted Soft-Bit-flipping Decoder is used to overcome such drawbacks of conventional algorithms. This research has been focused on the SRWSBF algorithm to reduce decoding latency, hardware complexity and power consumption as well as increasing the performance. The hardware complication of the SRWSBF algorithm can be considerably minimized by replacing difficult computations of the check nodes with simple summations and comparison operations. Simple Max likelihood test process is also considered at the variable nodes and it is computed at each variable node, which significantly reduces the latency and power consumption. Considering the above factors, the proposed work uses SRWSBF algorithm and focused on low complexity design of LDPC hardware architecture.

No. of Pages : 15 No. of Claims : 4

(12) PATENT APPLICATION PUBLICATION
(19) INDIA
(22) Date of filing of Application :23/12/2019
(21) Application No.201941053591 A
(43) Publication Date : 18/09/2020

(54) Title of the invention : AN EFFICIENT ARITHMETIC VLSI ARCHITECTURE FOR DWPT ERROR APPROXIMATION

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|---|---|
| (51) International classification | :H03H0017060000, H03H0017020000, G06F0007544000, G06F0007523000, G06F0017500000 |
| (31) Priority Document No | :NA |
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| (33) Name of priority country | :NA |
| (86) International Application No | :NA |
| Filing Date | :NA |
| (87) International Publication No | : NA |
| (61) Patent of Addition to Application Number | :NA |
| Filing Date | :NA |
| (62) Divisional to Application Number | :NA |
| Filing Date | :NA |

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(57) Abstract :
The power budget, size and cost make the task difficult to integrate more functions as the signal processing algorithms such as Discrete wavelet transform (DWT), Discrete wavelet packet transform (DWPT), finite impulse response (FIR) filtering. Therefore, developing low-complexity hardware efficient arithmetic design for healthcare application remains a challenge. DSP algorithms are implemented in dedicated hardware system to meet space-time requirement of resource constrained applications such as repetitive multiply-accumulate operations, computational symmetry and redundancy. Efficient implementation of multiplication operations is a key issue in digital filter design of DSP application. Separate approach is used for signed and unsigned multiplication. Approximate multiplication and addition operation provide small area and leakage power due to saving of storage data-bits. Approximation computation methodology produces dynamic power reduction due to memory access saving. Approximate computation consider small percentage of accuracy loss that does not affect much the overall application specific performance in digital arithmetic hardware design. Delay and power consumption is considered to be major issue in ripple carry adder (RCA) design is required to study the effectiveness of the arithmetic coefficient approximation method on DWPT computation. The bit level optimization of full-width adder tree for multiple constant multiplication (MCM) is given to taking the advantage of shifting operation. Considered images with different colour and edge information for DWPT applications are grouped as low-texture, moderate-texture and higher-texture images for discussion purpose. Less colour variation with less edge information refer to low-texture image, less colour variation with more edge information refer to moderate-texture image, and more colour variation with more edge information refer to higher-texture image. Pixel variation is more in data-vectors of higher-texture images, relatively less in data-vectors of moderate-texture images and almost absent/small in data-vectors of low-texture images. The proposed shift-add register (SAR) and approximate arithmetic architecture designs use a fixed-bias for error-compensation. The fixed-bias compensates truncation error near accurately for input data-vector with more pixel variation while overcompensate the truncation error for input data-vector with small pixel variation.

No. of Pages : 15 No. of Claims : 2

Australian Government

IP Australia

# CERTIFICATE OF GRANT

# INNOVATION PATENT

**Patent number:** 2020102448

The Commissioner of Patents has granted the above patent on 28 October 2020, and certifies that the below particulars have been registered in the Register of Patents.

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**Title of invention:**

EARLY COVID PREDICTION: NEURO FUZZY MULTI-LAYERED DATA CLASSIFIER

**Name of inventor(s):**

Ramana, Kadiyala; Kumar, Madapuri Rudra; Senthil Mahesh, P.C.; Prasanthi, B.; Hari Krishna, T.; Surya Narayana, G. and Kallam, Suresh

**Term of Patent:**

Eight years from 27 September 2020

NOTE: This Innovation Patent cannot be enforced unless and until it has been examined by the Commissioner of Patents and a Certificate of Examination has been issued. See sections 120(1A) and 129A of the Patents Act 1990, set out on the reverse of this document.

COMMONWEALTH OF AUSTRALIA AUSTRALIA PATENT OFFICE

Dated this 28th day of October 2020

Commissioner of Patents

(12) PATENT APPLICATION PUBLICATION
(19) INDIA
(22) Date of filing of Application :03/06/2020

(21) Application No.202041023333 A
(43) Publication Date : 12/06/2020

(54) Title of the invention : DIRECT CONTROL OF TORQUE OF INDUCTION MOTOR BASED ON FUZZY LOGIC APPLIED FOR ELECTRICAL VEHICLES

| | |
|---|---|
| (51) International classification | :B60W 20/00 |
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| (32) Priority Date | :NA |
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| (86) International Application No | :NA |
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| (87) International Publication No | : NA |
| (61) Patent of Addition to Application Number | :NA |
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(57) Abstract :
This invention investigates suitable mechanism for torque control method applicable for electric vehicle. Drive used in electric vehicle comprises of induction motor which are re-woundable and IGBT inverter of three level which switches at a frequency of 10 kHz. In this invention, novel technique of controlling direct torque is investigated with the presence of IGBT inverter consisting of three levels implemented by scheme of fuzzy logic control namely DTFC (Direct Torque Fuzzy Control) in combination with SVM (Space Vector Modulation). Simulation is done using Matlab Simulink and results are obtained. Comparison is done between various schemes of torque control of induction motor for Electric vehicle. From the simulation results it is clear that proposed invention of DTFC in combination with space vector modulation performs well compared to other techniques for the application of electrical vehicles.

No. of Pages : 2 No. of Claims : 6

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GOVERNMENT OF INDIA

Controller General of Patents,Designs and Trademarks
Department of Industrial Policy and Promotion
Ministry of Commerce and Industry

## Application Details

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| TITLE OF INVENTION | HTVM-BLOCK CHAIN SYSTEM: HEALTHCARE TRANSACTION VALIDATION AND MEDICAL OBSERVATION CARE USING BLOCK CHAIN SYSTEM. |
| FIELD OF INVENTION | COMPUTER SCIENCE |
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## Application Status

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# CERTIFICATE OF GRANT

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**Title of invention:**

EXPECTED CONDITIONAL CLUSTERED REGRESSIVE DEEP MULTILAYER PRECEPTED NEURAL LEARNING FOR IOT BASED CELLULAR NETWORK TRAFFIC PREDICTION WITH BIG DATA

**Name of inventor(s):**

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**Term of Patent:**

Eight years from 16 December 2020

COMMONWEALTH OF AUSTRALIA AUSTRALIA PATENT OFFICE

Dated this 17th day of February 2021

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PATENTS ACT 1990

The Australian Patents Register is the official record and should be referred to for the full details pertaining to this IP Right.

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# CERTIFICATE OF GRANT

# INNOVATION PATENT

**Patent number:** 2021103546

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**Title of invention:**

HYBRID NETWORK FOR REAL-TIME TRACKING USING MACHINE TO MACHINE COMMUNICATION

**Name of inventor(s):**

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