Annamacharya Institute of Technology & Sciences

Department of E.C.E.

IV-B.Tech ECE-A-Section Project Batches (2020-21)

Sl.No	Batch No.	Roll No.	Title
1.	**A1**	**17701A0404** **17701A0451** **17701A0432** **17701A0428**	Design of high performance voltage level shifter for IOT Applications
2.	**A2**	**17701A0431** **18705A0404** **17701A0459** **17701A0411**	Performance Evaluation of GDI Technique in domino based logic circuits using CMOS Technology
3.	**A3**	**17701A0422** **18705A0402** **17701A0452** **17701A0405**	Design of dual band cpw meander line fed Circular path antenna with CSRR slots for GPS and WLAN applications
4.	**A4**	**17701A0448** **17701A0438** **17701A0436** **18705A0403**	An Optimized low intensity Face Recognition using Deep Learning and Convolution Neural Network
5.	**A5**	**17701A0455** **17701A0413** **17701A0408** **17701A0426**	Design of Miniaturized Dual Band Microstrip Antenna for WLAN Applications
6.	**A6**	**17701A0443** **17701A0425** **17701A0419** **17701A0403**	Detection of Triple Riding and without Helmet riders using YOLOV2 Detector Algorithm
7.	**A7**	**17701A0412** **17701A0454** **17701A0440** **17701A0420**	Saliency Based image segmentation to analyze COVID-19 infected CTSCAN Images
8.	**A8**	**17701A0441** **17701A0456**	Power Analysis of LOG2 sub band encoding for wearable EEG Recorder

		17701A0435 **18705A0401**	
9.	**A9**	**17701A0444** **17701A0410** **17701A0423** **17701A0401**	A Novel Technique for Authentication using ECG
10.	**A10**	**17701A0442** **17701A0450** **17701A0417** **17701A0414**	Fixing DRC and LVS of the layout for sense amplifier
11.	**A11**	**17701A0430** **17701A0439** **17701A0458** **17701A0445**	Analysis of Nephropathy images using LPMPR filter and Morphological Watershed segmentation
12.	**A12**	**17701A0418** **17701A0457** **17701A0446** **17701A0434**	Lane Detection for Auto-pilot vehicles using perspective and Histogram approach
13.	**A13**	**17701A0447** **17701A0421** **17701A0407** **17701A0433**	Locker security system with image and voice Authentication
14.	**A14**	**17701A0416** **17701A0415** **17701A0424**	Design of low power high performance sense amplifier based Flip-flop using LECTOR Technique in 45nm CMOS Technology
15.	**A15**	**17701A0453** **17701A0449** **17701A0409**	High speed and area effective VLSI Architecture of three operand binary adder using Tanner EDA tool

IV-B.Tech ECE-B-Section Project Batches (2020-21)

S.No	Batch No.	Roll No.	Title
a.	B1	17701A04B1 17701A0491 17701A04A3 18705A0408	An Efficient Method for detection and classification of pulmonary and pancreatic Neoplasma based on deep learning
2.	B2	17701A0465 17701A0482 17701A0481 17701A04A0	Low power design of 4-Bit counter using digital switching circuits for counting applications
3.	B3	17701A0486 18705A0412 17701A04A6 18705A0409	Covid -19 fencing system contact traceability
4.	B4	17701A0470 17701A0467 18705A0411 17701A0485	Traffic management by monitoring wearher parameters and pollutants remotely using Rasberry Pi
5.	B5	17701A0479 17701A0468 17701A0471 17701A0498	Multi model medical image fusion using laplacian Re-decomposition framework
6.	B6	17701A0496 17701A04A2 17701A0483 18705A0410	Design of GDI Technique Based reversible Logic Combinational circuits
7.	B7	17701A04A7 18705A0407 17701A04A1 17701A0472	A Modified Gate diffusion input technique based proficient 4-Bit Priority encoder
8.	B8	17701A0499 17701A0494 17701A0487 17701A04A9	Design of reversible sequential circuits optimizing quantum cost, delay and garbage values

9.	B9	18705A0406 17701A0490 17701A0488 17701A04A4	Memory cell implementation using GDI Logic
10.	B10	17701A0480 17701A0476 17701A04A8 17701A0466	Aurdino security system
11.	B11	17701A0462 17701A0495 17701A0478 17701A0493	32-bit MAC unit design using vedic multiplier and reversible logic gate
12.	B12	17701A0469 17701A04B0 17701A0477 17701A0463	Advanced traffic violation controland penalty system with web server
13.	B13	17701A0474 17701A0460 17701A0484	Attendance evaluation with Face Recognition by using opencv
14.	B14	17701A04A5 17701A0473 17701A0464	Analysis of diabetic Nephropathy images using Kuwahara filter and Morphological watershed segmentation algorithm
15.	B15	17701A0461 17701A0492 17701A0497	A low power and high speed radix-4 booth multiplier

IV-B.Tech ECE-C-Section Project Batches (2020-21)

S.No	Batch No.	Roll No.	Title
1.	**C1**	**17701A04E8** **17701A04D4** **17701A04C1** **18705A0415**	DCTQ processor design using verilog
2.	**C2**	**17701A04B6** **17701A04C7** **17701A04C5** **17701A04F4**	Optimal Solution for VLSI physical design automation using Hybrid Genetic Algorithm
3.	**C3**	**18705A0414** **17701A04C4** **17701A04C2** **17701A04B8**	IOT based smart device for controlling home appliances using hand gestures
4.	**C4**	**17701A04D5** **17701A04D6** **17701A04E1** **18705A0417**	Design and implementation of low power, high performance of 2-4 and 4-16 mixed logic line decoders
5.	**C5**	**17701A04E0** **17701A04C9** **17701A04C6** **17701A04B5**	An Optimized Complex Motion Prediction Based Video Synopsis
6.	**C6**	**17701A04E6** **17701A04D2** **17701A04E5** **17701A04F0**	Design of low power, low noise current mirror OTA using 45nm technology
7.	**C7**	**17701A04F9** **17701A04G6** **17701A04E3** **17701A04D3**	Real time water quality monitoring system using IOT
8.	**C8**	**17701A04C0** **18705A0416** **17701A04G2** **18705A0418**	Internal Crack Detection In Cylindrical Concrete Using Ultrasonic Sensors

9.	**C9**	**17701A04G1** **17701A04G4** **17701A04F3** **17701A04D7**	High-Speed And Area Efficient Based Rounding Method In Dsp Applications
10	**C10**	**17701A04B4** **17701A04G5** **17701A04G0** **17701A04B7**	Retinal vessel tortuosity in fundus images
11	**C11**	**17701A04E2** **17701A04C8** **17701A04F6** **17701A04D9**	Fast fog removal technique using multiple exposure image fusion.
12	**C12**	**17701A04D8** **17701A04D0** **17701A04C3** **17701A04B3**	Deep Learning Based Food Detection Method at Restaurants For Automatic Billing
13	**C13**	**17701A04G3** **17701A04E4** **17701A04E7**	Low power high speed arithmetic circuit using full swing xor-xnor cells
14	**C14**	**17701A04F5** **17701A04B9** **17701A04B2**	Reliability enhancement of low power sequential circuits using reconfigurable pulsed latches

IV-B.Tech ECE-D-Section Project Batches (2020-21)

S.No	Batch No.	Roll No.	Title
1.	**D1**	**17709A0436** **17709A0426** **17709A0405** **17709A0417** **17709A0410**	DESIGN OF EFFICIENT CMOS FIR FILTER IN 45NM TECHNOLOGY
2.	**D2**	**17709A0431** **17709A0423** **17709A0424** **17709A0403**	INDEXING AND RETRIEVAL SYSTEM FOR SPEECH ANNOTATED DIGITAL IMAGES
3.	**D3**	**17709A0406** **17709A0412** **17709A0438** **17709A0421**	ADVANCED TCAM DESIGN USING SRAM
4.	**D4**	**17709A0435** **17709A0429** **17709A0404** **17709A0418**	DETECTION OF OPTIC DISC USING MORPHOLOGY BASED ALGORITHM
5.	**D5**	**17709A0437** **16709A0414** **17709A0433** **17709A0434**	IMAGE PROCESSING THROUGH VERILOG HDL
6.	**D6**	**17709A0430** **17709A0413** **17709A0428** **17709A0415** **17709A0401**	AREA AND POWER EFFICIENT STAIRCASE ENCODER IMPLEMENTATION FOR HIGH THROUGHPUT FIBER OPTICAL COMMUNICATION
7.	**D7**	**17709A0409** **17709A0402** **17709A0440** **17709A0411** **17709A0439**	DESIGN OF A 16BIT HARVARD STRUCTURED RISC PROCESSOR IN CADENCE 45NM TECHNOLOGY
8.	**D8**	**17709A0425** **17709A0416**	A HYBRID METHOD FOR VASCULAR ENHANCEMENT AND ARTERY SEGMENTATION ON 2D RETINAL IMAGES

		17709A0432 **17709A0419**	
9.	**D9**	**17709A0422** **17709A0408** **17709A0407** **17709A0427**	IMPROVED RADIX-4 AND RADIX-8 FFT ALGORITHMS USED FOR WIRELESS COMMUNICATION

Head of the Department